ROCKFORD INSTRUMENT LAB
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Rockford, IL 61108

62-5007

Instruction Manual

Cherry Electric

for

MODEL 1750

XTRA-FUNCTION 3-1/2 DIGIT DIGITAL MULTIMETER

DATA PRECISION
...years ahead

62-5007

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MODEL 1750

XTRA-FUNCTION 3-1/2 DIGIT DIGITAL MULTIMETER

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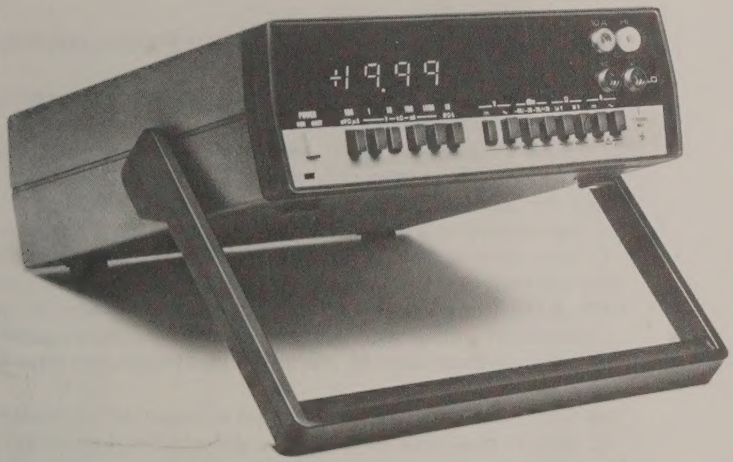

Frontispiece. Model 1750 3½ Digit Digital Multimeter

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Chapter 1
INTRODUCTION

1.1 GENERAL, SCOPE OF MANUAL

a. Data Precision Model 1750 Digital Multimeter is a 3½ digit, laboratory quality, portable as well as bench-useful, multimeter, incorporating 34 Measuring Function/Range capabilities. These include: DCV, ACV, DCmA, ACmA, KOhms (LoV), KOhms (HiV), dBm (−20 to +20) and dBm (−20 to −60). Resolutions of 100 microvolts, 0.1 ohms, and 100 nanoamperes are obtained at the lowest selectable full scale range while voltages up to 1000VDC or 1400 peak AC and currents up to 10 amperes may be measured by Model 1750 with 3½ digit resolution and specified accuracies. All ac measurements are displayed in TRUE RMS units, and all values are direct reading with automatically positioned decimal point and polarity sign (for dc and dB measurements only).

b. Information in this manual is organized so that operators and system users may locate applicable data and instructions (through Chapter 3) without having to wade-through technical detail necessary for maintenance and repair. Information in Chapters 4 and 5 essentially support the technical requirements for maintenance, trouble-shooting and repair activities.

c. This manual contains operating instructions and descriptions of field-installable options as well as of the basic instrument.

1.2 OPERATING FEATURES

Model 1750 Digital Multimeter provides the user with a number of unusual performance features. Among these are:

(a) **Laboratory Bench or Field Portability:** obtained by a built-in battery charger and a field-installable battery. The battery is always being recharged when the line cord is connected to the ac source, even while the instrument is not in operation (OFF).

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(b) **Easy-to-Read Display:** obtained by using bright, large (0.43 inch-high), LED's behind a non-reflective optical filter.

(c) **Easy-to-Understand Display Measurements:** Engineering units for direct-reading values are engraved directly above function selector pushbuttons. Automatic positioning of decimal point removes need for any further interpretive reading of displayed value. Polarity signs are displayed for dc and for dBm measurements. Blanking of digits for out-of-range signals prevents reading invalid displays.

(d) **Low-level Battery Monitoring:** Decimal point starts to blink when battery level drops to provide only 10 more minutes of operating power. 12-hour recharge cycle develops full charge for 6 hours of continuous operation. Blinking decimal point also indicates a very low ac line voltage when no battery is used.

1.3 SPECIFICATIONS

1.3.1 DC Volts

Nominal Range	Overrange	Resolution
±100.0 mVDC	±199.9	100μV
±1.000 VDC	±1.999	1mV
±10.00 VDC	±19.99	10mV
±100.0 VDC	±199.9	100mV
±1000. VDC	±1000.	1V

Input Impedance:
10MΩ, all ranges

Maximum Voltage:
±1000V, all ranges

Accuracy (1 year, 23°C, ±5°C):
±0.1% input ±1 l.s.d.

Temperature Coefficient (−10°C to +55°C, all ranges):
±.01% input/°C ±.01% range/°C

Common Mode Rejection Ratios (minimum)
with 1000Ω source impedance imbalance (AC line operation)
140dB at DC, >120dB at 50 and 60Hz

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Battery Operation:

At DC, so high as to be virtually unmeasurable.
At 50 and 60Hz, when in close proximity to ground (worst case): 120dB minimum

Common Mode Voltage:

500VDC (or peak AC) maximum when connected to AC power line. 1000VDC (or AC peak) maximum on battery operation (for safety).

Normal Mode Rejection Ratio:

60dB at 50Hz and 60Hz

1.3.2 AC Volts

Nominal Range	Overrange	Resolution
100.0 mVAC	199 9	100μV
1.000 VAC	1 999	1mV
10 00 VAC	19 99	10mV
100 0 VAC	199 9	100mV
1000. VAC	1000.	1V

Input Impedance:

10MΩ in parallel with 75pf or less

Sensing and Calibration:

True RMS

Accuracy (1 year, 23°C ±5°C):

20Hz: ±1% input ±5 l.s.d. (For ≥1% Range)
50Hz to 500Hz: ±0 4% input ±2 l.s.d. (For ≥1% Range)
2kHz: ±1.0% input ±2 l.s.d. (For ≥1% Range)
20kHz: ±3.0% input ±5 l.s.d. (For ≥ 20% Range)

(Interpolate between stated points to calculate accuracy at intermediate frequencies.)

Temperature Coefficient (−10°C to +55°C, all ranges):

20Hz to 500Hz: ±.02% input/°C ±.02% range/°C
2kHz: ±.1% input/°C ±.02% range/°C
20kHz: ±.15% input/°C ±.02% range/°C

(Interpolate between stated points to calculate intermediate temperature coefficients.)

Maximum Input Voltage (sinewave RMS):

20Hz to 10kHz: 1000V (1400V peak)
Above 10kHz: Do not exceed $V \times f(Hz) = 10^7$.

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Settling Time:
2.5 seconds maximum

Crest Factor:
5 at nominal range, 2.5 at 100% overrange

1.3.3 Resistance

Nominal Range	Overrange	Resolution	Nominal Test Current	
			HiV	LoV
100.0Ω	199.9Ω	100mΩ	1mA	1mA
1.000kΩ	1.999kΩ	1 Ω	1mA	200μA
10.00kΩ	19.99kΩ	10 Ω	200μA	20μA
100.0kΩ	199.9kΩ	100 Ω	20μA	2μA
1000.kΩ	1999.kΩ	1kΩ	2μA	200nA
10.00MΩ	19.99MΩ	10kΩ	200nA	20nA

Accuracy (1 year, 23°C ±5°C):

High Excitation

100.0Ω:	±0.2% input ±2 l.s.d. ±100mΩ
1.000kΩ–100.0kΩ:	±0.1% input ±1 l.s.d.
1000kΩ:	±0.1% input ±1 l.s.d.
10MΩ:	±0.2% input ±1 l.s.d.

Low Excitation

100.0Ω:	±0.1% input ±1 l.s.d. + 100mΩ
1.000kΩ–100.0kΩ:	±0.2% input ±2 l.s.d.
1000kΩ:	±0.3% input ±2 l.s.d.
10MΩ:	±1.0% input ±2 l.s.d.

Temperature Coefficient (−10°C to +55°C)

High Excitation

100.0Ω–100.0kΩ:	±.01% input/°C ±.01% range/°C
1000kΩ:	±.01% input/°C ±.01% range/°C
10MΩ:	±.02% input/°C ±.02% range/°C

Low Excitation

100.0Ω–100.0kΩ:	±.01% input/°C ±.01% range/°C
1000kΩ:	±.02% input/°C ±.02% range/°C
10MΩ:	±.1% input/°C ±.1% range/°C

Maximum Open Circuit Voltage:
(High Excitation) 2.5 Volt
(Low Excitation) 300mV

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Maximum Input Voltages:
440V RMS AC or DC for 5 seconds
250V RMS AC or DC, continuously

Settling Time:
100.0Ω to 1000kΩ: 1 second
10MΩ: 4 seconds

1.3.4 DC Current

Nominal Range	Overrange	Resolution
100.0μA	±199.9μA	0.1μA
1.000mA	±1.999mA	1μA
10.00mA	±19.99mA	10μA
100.0mA	±199.9mA	100μA
1000.mA	±1999.mA	1mA
10.00 A	±10.00 A	10mA

Maximum Current:
Series 2A fuse (250V) (10A range not fused)

Nominal Full Scale Voltage across Shunts:
100mV

Accuracy (1 year, 23°C ±5°C):
±0.3% input ±1 l.s.d. for 100μA to 1000mA
±0.5% input ±1 l.s.d. for 10A

Temperature Coefficient (−10°C to +55°C)
±0.02% input/°C ±0.01% range/°C

1.3.5 AC Current

Nominal Range	Overrange	Resolution
100.0μA	199.9μA	0.1μA
1.000mA	1.999mA	1μA
10.00mA	19.99mA	10μA
100.0mA	199.9mA	100μA
1000 mA	1999 mA	1mA
10.00 A	10.00 A	10mA

Maximum Current:
Series 2A fuse (250V) (10A range not fused)

Nominal Full Scale Voltage across Shunts:
100mV RMS

Sensing and Calibration:
True RMS

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Accuracy (1 year, 23°C ±5°C):

100.0μA–1000mA	20Hz:	±1.5% input ±5 l.s.d.	(For ≥1% Range)
100.0μA–1000mA	50Hz–10kHz:	±0.75% input ±2 l.s.d.	
100.0μA–1000mA	At 20kHz	±3.0% input ±2 l.s.d.	(For ≥20% Range)
10A	20Hz–1kHz (Max. freq.):	±1.5% input ±2 l.s.d.	(For ≥1% Range)

Temperature Coefficient (−10°C to +55°C)

100.0μA–1000mA	20Hz to 10kHz:	±0.03% input/°C ±0.02% range/°C
100.0μA–1000mA	At 20kHz:	±0.1% input/°C ±0.02% range/°C
10A	20Hz to 1kHz:	±0.15% input/°C ±0.02% range/°C

(Interpolate between stated points to calculate intermediate temperature coefficients.)

1.3.6 dBm

Ranges:

−60dBm to −20dBm
−20dBm to +20dBm

Frequency:

20Hz to 20kHz

Accuracy:

±1dB (referenced to 600Ω) for frequencies and ranges in table below.

Frequencies	dB Reading	
	Low Scale	High Scale
20Hz to 3kHz	−60 to −20	−20 to +20
20Hz to 10kHz	−48 to −20	−8 to +20
20Hz to 20kHz	−42 to −20	−2 to +20

Max Input Voltage: 1000 V DC or AC RMS
Input Impedance: 10MΩ

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1.3.7 Functional Characteristics (AC & DC Measurements)

Reading Rate:
2.5 readings/second

Polarity:
Autopolarity

Overload Indication:
Blanking of all digits leaving sign (if applicable) and decimal point illuminated.

Low Battery Indication:
Decimal point blinks when less than 10 minutes of battery operation remain. If no battery, blinking indicates excessively low line voltage.

Overrange:
100%, except on 1000V ranges, dB ranges, and 10A range

Power Less than 2.5W (without battery assembly)
AC source of 115 ± 10VRMS, 47 to 63Hz.
100 ± 10VRMS, 47 to 63Hz
230 ± 20VRMS, 47 to 63Hz.
6 NiCd battery assembly (accessory)
Built-in charger (standard)

Display:
Three 0.43" LED Full Decade
One 0.43" LED Polarity and Most Significant Digit
Decimal points in each decade

Size:
8 1/2" W × 9 7/8" D × 2 7/8" H (including handles)

Weight:
2.5 pounds without battery; 3 pounds with battery. 5 pounds shipping

1.3.8 Environment

Temperature Range	with Battery Option Installed
Operating, −10°C to +55°C	0°C to 40°C
Storage, −40°C to +80°C	−25°C to +50°C

Humidity:
80% RH maximum, 0°C to 40°C, non condensing
70% RH maximum 40°C to +55°C " "

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1.3.9 Digital Input/Output (For BCD Option) Signal (Functions)

All levels with respect to COMMON digital (ground)

DATA: (out)	13 lines; 3 BCD digits and 1 MSD, positive True logic.
SIGN: (out)	1 line; High level indicates positive polarity
$\overline{\text{OVLD}}$: (out)	1 line; Low level indicates input, when scaled for selected range ac, dc, or Ω is greater than 1999 counts. For dBm measurements, OVLD goes low at approximately 5dBm above and below selected modes (−20 to +20dBm or −60 to −20dBm).
DATA READY: (out)	1 line; High level is present when BCD data lines have been updated. Low level is present when BCD data lines are being updated.
$\overline{\text{HOLD}}$: (in)	1 line; Low level input retains last converted value on output data lines. Model 1750 continues to digitize and display the input signal at the nominal trigger rate of 2.5 per second.
DECIMAL POINT: (out)	4 lines; High level indicates the selected range scale.

1.4 OPTIONS AND ACCESSORIES

Model 1750 Digital Multimeter may be ordered with any one of three field-installable and/or one factory-installed options. In addition, Model 1750 applications may be extended by using any of a number of accessories.

a. Field-Installable Options

High-Efficiency LED Display (quadruples light output without additional current drain)	HL1
Opto-Isolated BCD Output	BCD1
Rechargeable Battery Assembly	C48

b. Factory-Installed Option

Rear Input Connector	IC1

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ORDERING GUIDE

For Line Voltage (47–63Hz)	Specify
105–125 VAC	Model 1750
210–250 VAC	Model 1750E
90–110 VAC	Model 1750J

c. Accessories

*Test Leads	T5
Rack Mount (L, R or Dual)	RMD1
High Voltage Probe (to 40KV) DC	V41A
Current Probe (to 150 Amp AC (30–400 Hz))	IP151
*Line Cord	L45
Deluxe Test Lead Accessory Kit	TX
Current Probe (10 to 1000 Amp AC)	IP1001
Peak Detector Probe	RF471
Hooded BCD Output Connector	HC1
BCD Output Connector, less Hood	A6

*One set included at no charge as part of basic ordering configuration.

Specify Options and Accessories as identified above.

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Chapter 2
OPERATION

NOTE:
Read this chapter carefully before attempting to use your Model 1750 DMM. Retain these instructions. Observe all WARNINGS and CAUTIONS.

2.1 GENERAL

a. Chapter 2 contains detailed instructions for connecting and operating the Model 1750 DMM, including safety precautions to prevent damage to personnel or equipment. In addition, the chapter contains some application notes designed to assist users to obtain valid measurements in harsh environments. Refer to the specifications in paragraph 1.3 to obtain the tolerance with which displayed measurements may be interpreted.

b. Safety Markings The front panel incorporates two standard operator warnings. The significance of each is:

⚠ Located between terminals "10A" and "HI".

This advises the operator to refer to the instruction manual before using these terminals.

Located to the right of terminal "HI".

This warns the operator that there may be dangerously high voltage at this location, or that there is a voltage limitation to be considered when using this terminal.

The rear panel mounts a standard grounding lug, electrically connected to the "ground" terminal of the 3-wire line cord receptacle in the rear panel.

2.2 UNPACKING & REPACKING

a. Figure 2-1 identifies the components of the packaging configuration for Model 1750 DMM. As shown in that illustration, the multimeter is

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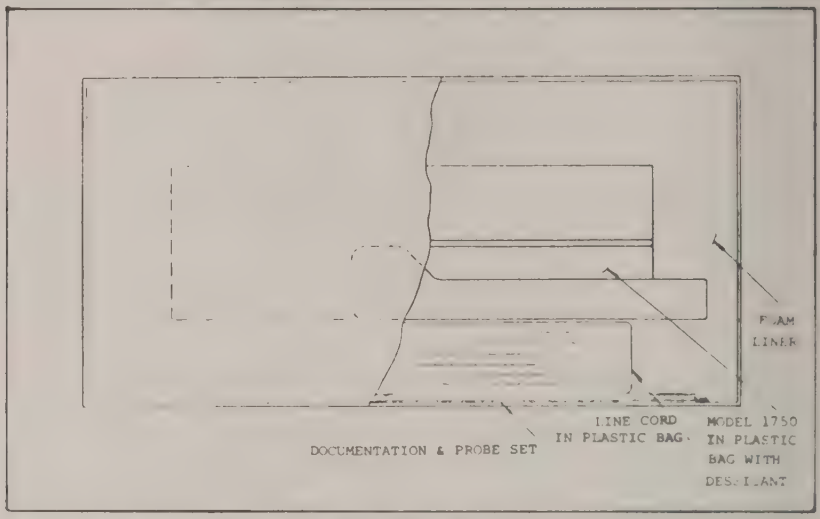

Figure 2-1 — Model 1750 Packing Configuration

placed in a waterproof plastic wrapper, securely fitted between molded-foam shock isolators, and placed with the documentation in its shipping carton. When unpacked, you should find:

(1) Model 1750 DMM
(2) Line Cord
(3) Test Probe Assembly & Alligator Clips
(4) Certificate of Conformance
(5) Warranty Card
(6) Factory Test Data Sheet
(7) Spare 2A 250V 3AG Fuse, F301

b. Carefully examine these articles, noting especially the matching serial numbers of the instrument and the test data. Inspect the packing case and the instrument for any signs of damage during shipment and report immediately to the carrier. Fill out and return the warranty card to register your instrument and to establish your warrantied service interval

c. Accessories, such as spare leads or high voltage probes, may have been ordered. These will be shipped in their own containers. The battery assembly and or other field installable options, if ordered with meter, will be installed prior to shipment.

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d. Retain the packing material for reshipment.

e. When shipping Model 1750 DMM, place the instrument in its protective carrying case including test probes and line cord. Use foam liners and pack in original shipping carton, if available.

f. If the Model 1750 DMM is to be kept stored without use for any appreciable time (6 months or more) and a battery assembly is installed, the battery should be recharged every 6 months.

2.3 FRONT PANEL CONTROLS & INDICATORS

Figure 2-2 and Table 2-1 identify and describe operating features at the front panel of the standard Model 1750 Digital Multimeter.

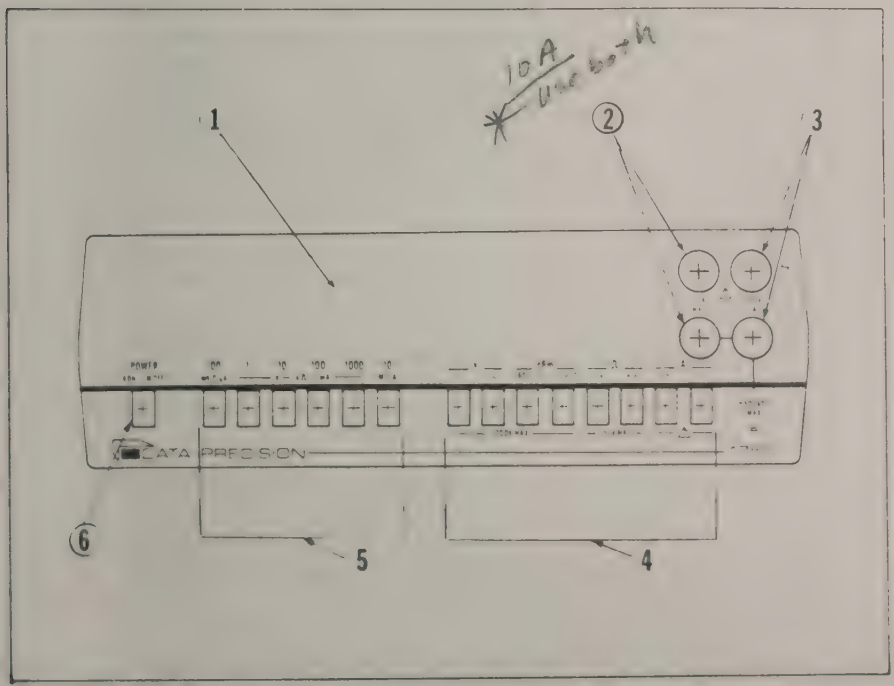

Figure 2-2 — Model 1750 DMM Front Panel Features

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Table 2-1
FRONT PANEL OPERATING FEATURES (Fig. 2-2)

Fig. Ref.	Name, Description	Function
1	Display (0.43" LED) (Bright display available as option)	3 full decades, MSD "1", polarity (+, −), and decimal point. Direct reading in units determined by function and range selection.
2	10A (J401, J402) (J402 is internally connected to LO, J403)	Two banana plug connectors (input and return), for high current input signals up to 10 amperes. Return connected internally to LO.
3	HI (J400) LO (J403)	Two banana plug connectors (high and return), for all input signals except for currents greater than 2 amperes. Input voltages up to 1000 volts. Low side may be up to ±500 VDC above case ground. Polarity of signals is that of HI with respect to LO terminals.
4	Function Selectors	8 interlocked pushbuttons, with panel markings identifying the measuring function for each.
5	Range Selectors	6 pushbuttons, with panel markings identifying the selected range scale. Range selection automatically positions the decimal point.
6	POWER ON-OFF	Push-push switch applies power to meter circuitry. Power may be furnished by battery or AC mains, as determined by use of line power cord (See Table 2-2).

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2.4 REAR PANEL FEATURES

Figure 2-3 and Table 2-2 identify and describe features at the rear panel of Model 1750 Digital Multimeter.

Table 2-2
REAR PANEL OPERATING FEATURES (Fig. 2-3)

Fig	Name/Description	Function
1	Rear Input Connector (J302) (Option) (Factory-installed)	7-terminal circular plug connector with parallel input circuit connections to front panel.
2	Fuse (F300)	1/16-Ampere 250V Fast Blow 3AG line fuse.
3	Receptacle for Line Cord (J300)	3-prong receptacle for ac line cord
4	Ground (J301)	Binding post for line ground.
5	PC-Board Edge Connector (Option)	22-position dual readout edge connector for Digital Data, Status, and control signals when BCD option is installed
6	Fuse (F301)	2A, 250V, Fast Blow 3AG fuse in series with current measurement input (except for 10A).

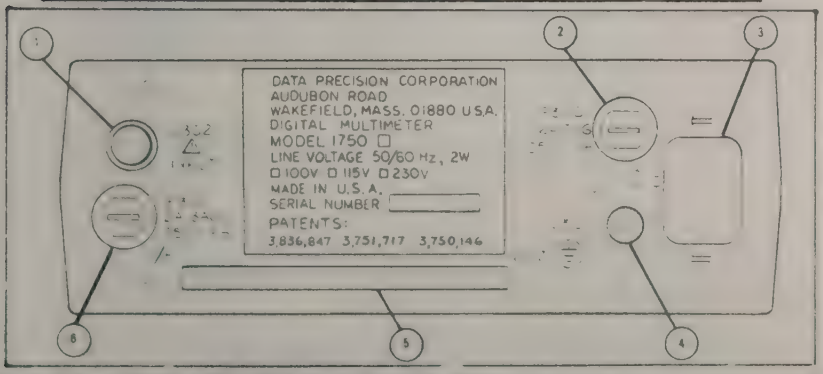

Figure 2-3 — Model 1750 DMM Rear Panel Features

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2.5 OPERATION

2.5.1 Powering

a. Model 1750 Digital Multimeter is powered by 115VAC (Model 1750) or 230VAC (Model 1750E) or 100VAC (Model 1750J) as determined by the ordered configuration. (See rear panel label.) Connect the line cord to the rear connector (Figure 2-3, item 3) and to the power source. In addition, any Model 1750 may be powered by an accessory battery assembly, C48, field-installable in guides within the case. When a battery assembly is installed, it is always being recharged when the ac power is connected.

b. Turn on power by operating the switch (Figure 2-2, item 6).

c. Voltage output of an installed battery assembly is monitored (when the power switch is turned ON) by standard internal circuitry, and a low-level battery output is indicated by a blinking decimal point in the display. A completely charged battery assembly will supply 6 hours of trouble-free performance, and 12 recharging hours will fully charge a completely discharged battery assembly. In absence of battery, blinking decimal point indicates an excessively low line voltage source.

d. The multimeter may exhibit certain battery performance below rated characteristics that are only temporary operational effects typical of battery usage patterns. Such below-specification performance can be corrected easily and in a minimum of time.

Memory. If the meter is used in a series of repeated partial charge and discharge cycles that use only a small portion of the available battery capacity, the battery will become conditioned to delivery only slightly more than normal end-of-discharge voltage capacity when called on to perform in an extended discharge cycle.

To correct this condition, subject the battery to a deep discharge, and then recharge to full capacity. This will erase the "memory" pattern.

Sustained Overcharge. If the meter is kept on "high voltage charge" for long periods of time without discharge interruptions, the battery may not deliver normal voltage at the end of the first sustained discharge operation thereafter.

To correct, proceed as for the memory effect described above: discharge the battery, then recharge to full capacity.

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2.5.2 Signal Connections

WARNING

Inputs applied through rear-panel connector are paralleled to front panel plugs. Check for any rear inputs before making any front-panel connections. Remove any rear panel connections before using front-panel inputs, and vice-versa.

a. A pair of test leads are furnished as standard accessories with each ordered Model 1750 Digital Multimeter. A banana plug connector at one end mates with the Model 1750 Digital Multimeter front panel input connector, while the probe end of each lead may be configured for spade lug contact. Alligator clip adaptors are furnished at no additional charge with each standard test lead set.

b. When measuring with a Model 1750 Digital Multimeter that is connected to ac power, it is important to minimize ground loops that may introduce noise into the input circuit. (See applications data, paragraph 2.6).

c. Input terminals (Figure 2-2, Item 3) are used as the front panel connector pair to measure voltages up to 1000 volts, currents up to 2 amperes, resistances up to 20 Megohms, and dBm in the ranges -20 to +20 or -20 to +60. For currents greater than 2 amperes but not more than 10 amperes, the 10A terminals (Figure 2-2, item 2) must be used. The rear connector, J302, (factory-installed) parallels the front panel inputs and extreme caution should be used with these connections.
See WARNING at start of paragraph 2.5.2.

CAUTION

Before connecting the Model 1750 DMM to the unit under test, be sure that the values would not exceed the limits indicated on the front panel.

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d. Connect leads to Model 1750 DMM and to the unit under test.

e. Rear Input Connector (Option) When the rear connector option is installed, its terminal connections are as illustrated in Figure 2-4.

2.5.3 Selecting a Measuring Function

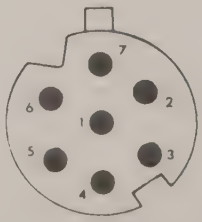
Select one of 8 measuring functions by operating the appropriate push button (Figure 2-2, item 4). The push buttons are interlocked so that operating any one will release any other one.

2.5.4 Selecting Range

a. Operate the pushbutton for a range scale expected to exceed the highest value expected. If an out-of-range indication appears in the display, choose the next higher range until an in-range value is displayed. If the first range selection results in a display of less than 190 counts, a greater resolution may be obtained by choosing the next lower range scale.

b. For ac or dc voltage, the highest range is 1000; the lowest is 100mV. For resistance measurements, the highest range is 10MΩ; the lowest is 100Ω. For ac or dc currents, the highest range is 10A; the lowest is 100μA. The dBm function and range are not independent; the range scale is automatically selected for each of the two available dBm selections.

J302



J302	SIGNAL NAME	FRONT PANEL
1	Input Signal (+)	J400 (HI)
2	Input Signal (–)	J403 (Lo)
*3	Input 10 Ampere Source	J401 (10A) (+)
4		
*5	Input 10 Ampere Return	J402 (10A) (–)
6		
7	Shield	

* Connect in parallel at input end of cable also.

Figure 2-4 — Rear Panel Signal Connections

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2.5.5 Reading the Display

a. The display is direct reading in the engineering units selected by the range scale (mV, V, μA, mA, A, Ω, kΩ, MΩ, and dBm) with automatic positioning of the decimal point. Polarity for dc and dBm measurements is indicated to the left of the most significant digit; no sign is indicated for any ac or ohms measurements. If the input signal exceeds the selected range scale, the digits will be blanked, the decimal point and the polarity sign (if appropriate) will remain lighted. A blinking decimal point indicates a low battery, or, in absence of battery, a low line voltage. See paragraph 2.5.1.

b. Table 2-3 illustrates the interpretation of a number of different displays in terms of the operated pushbuttons at the time.

c. True RMS and Crest Factor Model 1750 DMM displays the True RMS value of any input waveform, within a tolerance band specified for the frequency content of the input, the crest factor of the complex waveform, and the temperature of the operating environment. A crest factor of 5 signifies that the ac to dc converter remains a linear device (no distortion of output) for waveforms where the ratio of the peak to RMS is less than 5:1.

2.6 APPLICATION NOTES

2.6.1 General

Optimum performance is obtained from your Model 1750 DMM by observing a number of precautions in establishing the test measurement conditions. The few hints included in these paragraphs are only indicative of the types of measuring environment problems which may influence the meter performance. It is suggested that the user record his own application aids as he determines them.

2.6.2 Avoiding Ground Loops (Making Grounded Measurements)

If the line cord is connected, a potential difference may exist between the "ground" of the power source and the "ground" of the measured circuit. This difference of ground potentials may set up ground-loop currents and affect the measured values although the instrument will reduce their effects significantly (CMRR = 120dB, NMRR = 60db). The ground loop effects can be avoided almost completely by operating the meter on batteries.

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Table 2-3
TYPICAL MEASUREMENTS WITH MODEL 1750

Selected Measuring Function	Selected Range	Display	Interpretation
DCV	1	- 1.234	HI input is 1 234 volts more positive than LO input.
	100mV	123 4	HI input is 123.4 millivolts less positive than the LO.
	100V	- 123 4	HI input is 123 4 volts more positive than the LO input.
	100V	- .	HI input is more than 199.9 volts more positive than LO input.
ACV	100 100mV	123.4 123.4	AC input is 123.4V RMS. AC input is 123.4mV RMS.
dBm (−60/−20)	*	23.4	Input signal voltage between HI and LO is 23.4dB less than 1 milliwatt, referred to 600Ω.
kΩ(Lo)	10 10M	12.34 12.34	Resistance is 12.34 kilohms. Resistance is 12.34 Megohms.

*Range is not effective when dBm function is selected.

2.6.3 Making "Floating" Measurements

In a floating measurement such as in Figure 2-5, it is possible to introduce a common mode voltage by reactive coupling through the AC power line when that source of power is connected As in paragraph 2.6.2 although this effect is small, it may be avoided almost completely by disconnecting the AC power source and reverting automatically to battery power.

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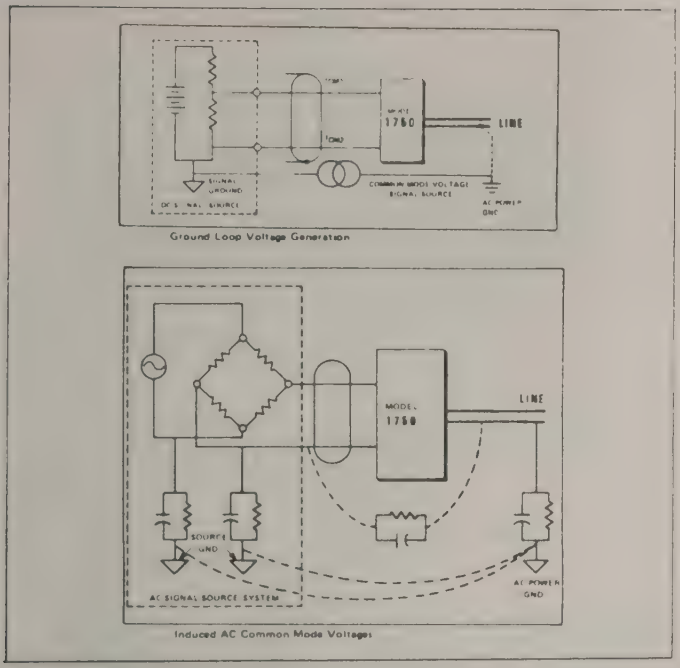

Figure 2-5 — Avoiding Ground Loops

2.6.4 Making High Resistance Measurements

a. When making measurements of very high impedance sources, as when required to measure resistance on the 10MΩ range, the input circuit may be susceptable to noise. The effect of voltage-producing noise fields on the probe leads may be sufficient to introduce significant changes in the least significant digit of the display

b. Measurement errors may be kept to a minimum under these circumstances by keeping the lead as short as possible (do not use any extensions on the probes), and by twisting the probe leads so as to equalize any field effects on the signal input leads.

NOTE:

It is good practice to twist probe leads whenever possible in order to equalize any field effects on the signal input leads

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2.6.5 Making Very Low Voltage Measurements

Problems may arise when measuring very low voltages because of the differences in temperature of the probe contact points. Both probes are plated brass, and if the HI probe is in contact with copper in a high ambient temperature (for example, in a computer tape drive mechanism), while the LO probe is grounded at a very much cooler steel cabinet frame, then a difference in emf of several hundred microvolts may result, changing the least significant digit. In order to minimize such errors, connect the probes wherever possible at approximately the same temperature.

2.7 OPERATOR SERVICING

a. Operator servicing of Model 1750 DMM is limited to replacement of fuses, and installation of accessory rechargeable battery assembly.

WARNING

Unplug line cord from ac source and from Model 1750 DMM before attempting to replace fuse or install battery assembly.

b. Fuse Replacement Table 2-4 identifies the fuse data, while Figure 2-3 indicates their location in the rear panel. To replace, unscrew fuse holder; remove spent fuse; replace in fuse holder; screw into panel.

c. Battery Installation Battery assembly, C48, is installed by sliding the battery case into the vertical channels on the interior rear panel. Contact is made with two clips mounted on the main board behind the rear panel. To install, remove top cover by removing two top screws in rear panel, lift top cover rearward and slide out; install battery assembly.

Table 2-4
FUSE REPLACEMENTS

Ref. Designation	Description	Function	Data Precision Part Number
F301	2A 250V 3AG	Protection for high current inputs on ranges from 100μA to 2A.	25-500002
F300	1.16A 250V 3AG	Line Fuse. Protection for power shorts.	25-500008

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Chapter 3

CALIBRATION

3.1 GENERAL

a. The Model 1750 Digital Multimeter is factory calibrated and burned-in prior to shipment, and is designed to remain in calibration for a minimum of 1 year before the recalibration procedure should be required. The complete set of factory test data sheets for each instrument is shipped with the meter and should be referenced to determine the need for calibration.

b. Once calibrated, Model 1750 DDM does not require any **operating zero** adjustment on any measurement function or any range scale, and no front panel adjustment is provided.

3.2 CALIBRATING ADJUSTMENTS

a. The adjustments to calibrate Model 1750 DMM are accessible after removing the top cover of the case. Table 3-1 identifies the adjustments and their function. To remove the cover, remove the two top screws in the back plate, lift the top rearward from the front bezel, and slide out Figure 3-1 indicates the major assemblies within the case, and Figure 3-2 points out the adjusting components listed in Table 3-1. Their reference designators are screened on the main circuit card.

b. When calibration is required, test standards of the ranges and accuracies listed in Table 3-2 should be used to eliminate any test standard uncertainty.

3.3 CALIBRATION PROCEDURES

a. Allow the instrument to warm up for one-half hour before beginning the recalibration.

b. Perform the adjustments in the sequence of Table 3-3. Apply test input standards of amplitude and frequency as close as possible to the values listed. Adjust the designated control until the display is the input

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(or the designated reading). If available test standards do not develop the listed values, then the closest value to the specified input should be used and the control adjusted accordingly. It is desirable to use signals at least 50% of the full scale value for the specified range.

c. When calibration is complete, reassemble the unit by replacing the top cover in reverse sequence of paragraph 3.2.

Table 3-1

CALIBRATION ADJUSTMENTS

Ref. Designation	Name	Function
R53	0.1V	Adjusts level of REFERENCE voltage for Phase 3 of A/D converter.
R59	0 04V	Adjusts level of offset adjustment for dBm measurement.
R22	RMS ZERO	Adjusts zero balance of TRUE RMS AC/ DC converter.
R25	RMS GAIN	Adjusts Scaling of TRUE RMS AC/DC converter.
R19	dBm ZERO	Adjusts zero balance of dBm converter.
R27	dBm GAIN	Adjusts scaling of dBm converter
C49 C4 C7 C12	AC Response	Adjusts input scaling circuit for frequency response over input range.

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Table 3-2

CALIBRATION TEST STANDARDS

PARAMETER	RANGE	ACCURACY TOLERANCES
DC VOLTAGE	0 TO 200.0MV	± 0.01%
AC VOLTAGE @ 500HZ @ 2.5KHZ	0 TO 200.0 MVRMS 0 TO 1000VRMS	± 0.05% ± 0.10%

Table 3-3

CALIBRATION SEQUENCE

STEP	FUNCTION SELECT	RANGE SELECT	TEST INPUT	ADJUST
1	DCV	100mV	+ 190.0mV	R53 TO + 190.0
2	ACV	100mV	500HZ 1.0mVRMS	R22 TO 01.0
3	ACV	100mV	2.5KHZ 100.0mVRMS	R25 TO 100.0
4	ACV	100	2.5KHZ 100.0VRMS	C49 TO 100.0
5	ACV	1K	2.5KHZ 1000.0VRMS	C12 TO 1000
6	ACV	10	2.5KHZ 10.00VRMS	C7 TO 10.00
7	ACV	1	2.5KHZ 1.000VRMS	C4 TO 1.000
8	REPEAT STEPS 4-7			
9	dBm + 20 20	N A	2.5KHZ 774.6mVRMS	R19 TO + 00.0
10	dBm + 60 20	N A	2.5KHZ 7.746mVRMS	R59 TO 40.0
11	dBm 60 20	N A	2.5KHZ 77.46mVRMS	R27 TO 20.0

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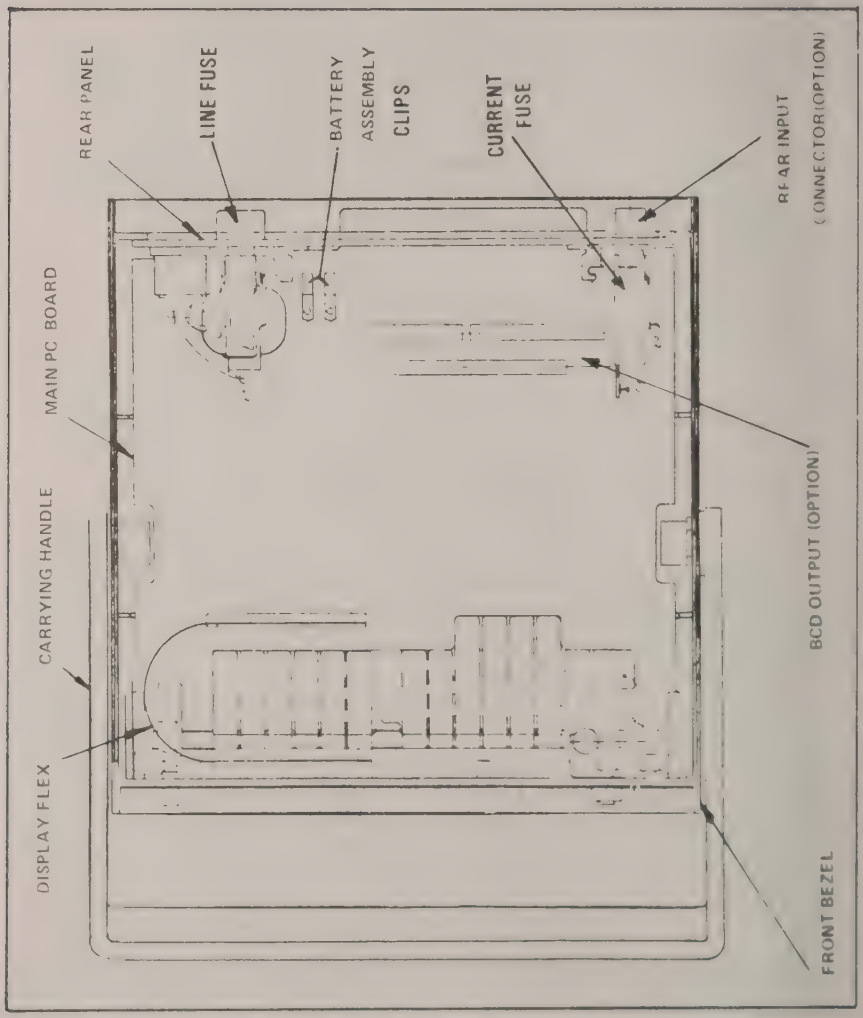

Figure 3 1. Model 1750 DMM Assemblies (Top Cover Removed)

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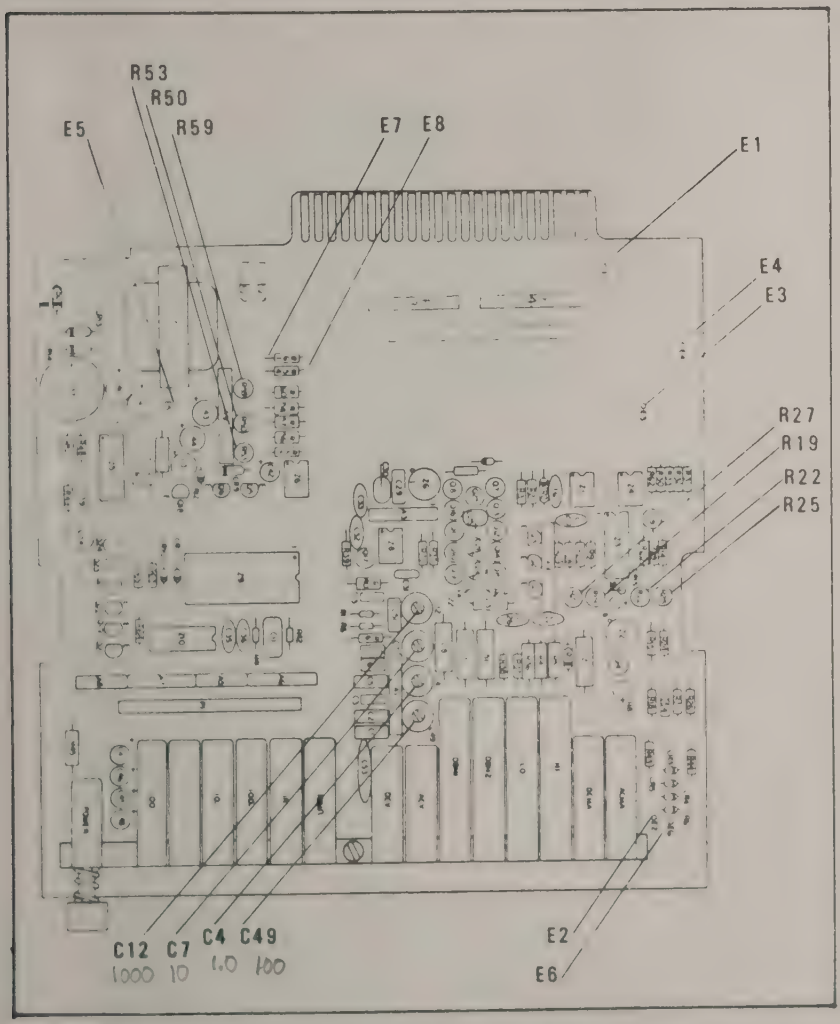

Figure 3-2. Location of Calibration Adjustments and Test Points

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NOTES:

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Chapter 4
PRINCIPLES OF OPERATION

4.1 GENERAL

a. Model 1750 Series Digital Multimeter converts input signals into digital displays using the integrating dual slope technique in a patented Tri-Phasic™ A D converter circuitry, employing Iso-Polar™ referencing and Ratiohmic™ circuit configuration for resistance measurements.

b. The multimeter is triggered internally to initiate a 3-phase measurement cycle. During Phase 1 the meter circuits are automatically servoed to determine the correction for the accumulated zero offsets in the analog integrator loop. In Phase 2 the signal to be measured, which has been conditioned according to the type of signal (AC, DC, Ohms or dBm) and selected range scale, is connected in series with the zero offset correction to the dual slope A D converter integrator which integrates the conditioned input for a fixed time interval of 100 milliseconds. After the fixed time interval of Phase 2, Phase 3 begins, in which the input signal is disconnected from the A D converter, and in its place a reference signal of opposite polarity and fixed magnitude is connected in series with the zero offset correction. The integration of the reference signal continues in Phase 3 until this second ramp of the dual ramp A D converter reduces the voltage at the integrating output to zero. The zero level is sensed and indicates the End of Conversion (EOC) if it occurs in 200 msec or less during Phase 3. If there has not been an EOC signal within 200 msec in Phase 3, the meter interprets this as an overload condition. The meter reduces the remaining voltage at the integrator output via a fast time discharge and at EOC initiates Phase 1 to restart the conversion cycle. The fast capacitor discharge circuit assures that the auto-zeroing integration in Phase 1 will start from zero conditions after an out-of-range input, and that there is no residual voltage offset at that time. The overload sense circuit also initiates the development of logic control signals for the overload display.

4.2 OVERALL BLOCK DIAGRAM & SYSTEM TIMING

As shown in Figure 4-1, Model 1750 DMM consists of essentially five main functional groups.

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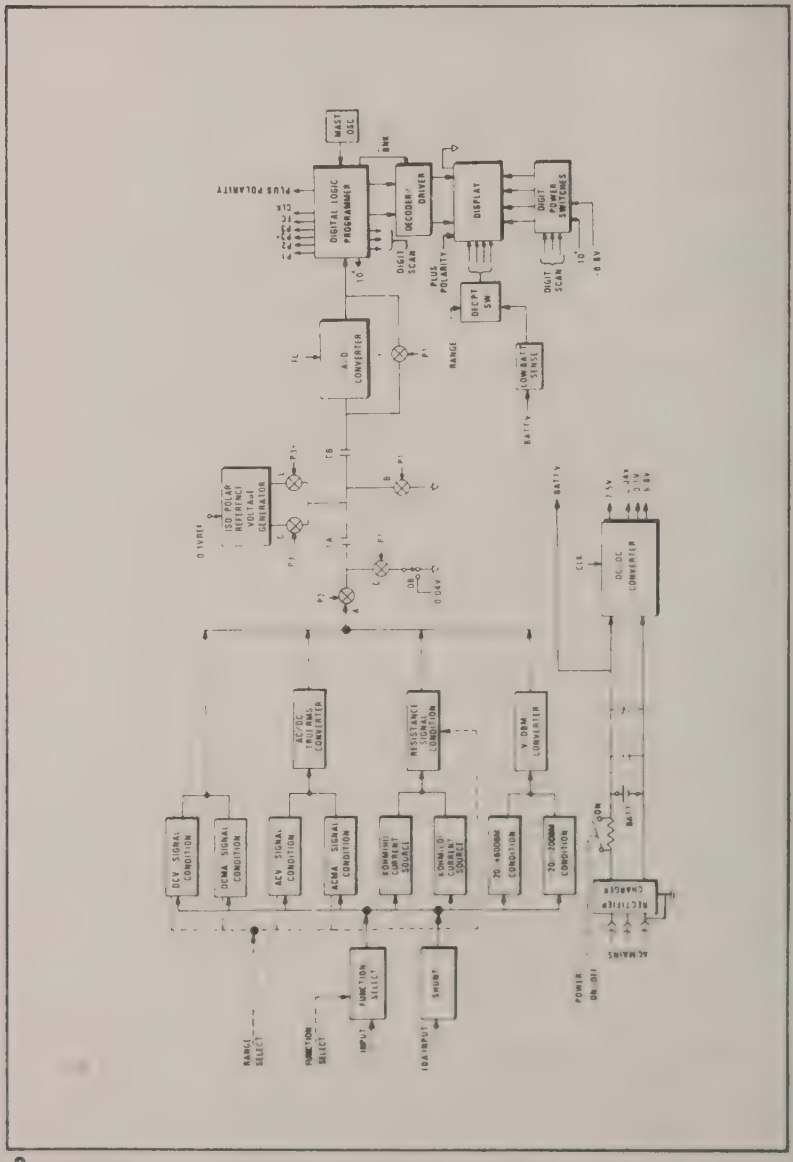

Figure 4-1. Model 1750 DMM System Block Diagram

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Input Signal Conditioning
Tri-Phasic A/D Converting
Digital Logic Programming
Decoder Driving and Displaying
Power Supplying

This paragraph briefly describes the functions performed in each major group, and is followed by circuit descriptions of each one

4.2.1 Input Signal Conditioning

The function of the input signal conditioning circuits is to transform the analog input signal to a dc voltage and to scale its magnitude so that 100 millivolts will result in 1000 counts on the display for ac and dc measurements. For dc voltage inputs, this requires only a scaling operation For dc currents, this requires both a conversion to voltage and a scaling operation while for ac inputs the conditioning also requires an ac to dc conversion of the scaled input.

The conditioning for resistance measurements requires the generation of a dc voltage signal proportional to the unknown resistance and this is accomplished in either of two modes, depending upon whether the measuring application permits a high voltage, KΩ(HiV), or is restricted to a low voltage, KΩ(LoV), to be applied across the unknown resistance In the first instance, up to 2 5 volts may be applied, and in the second, up to 300 millivolts may be applied across the resistance. The patented Ratiohmic circuitry develops the reference voltage for the reference integration phase by using the same current that flows through the unknown resistance to develop the reference voltage across a standard resistance

The ac dc Converter used to condition ac input signals is an IC component that also performs the logarithmic conversion for dBm measurements Its internal scaling develops 3mV per dB, and the signal conditioning for dBm inputs includes a biasing by 0 04V to obtain the correct range of direct reading values for the display in the 60 20dBm mode

Figure 4-1 also illustrates the separate signal conditioning for high current inputs up to 10 amperes This input is converted to a proportional voltage by a very low resistance shunt scaled for 10-ampere full scale, and then through the ac-to-dc converter (for ac inputs) or directly to the A D converter (for dc inputs).

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4.2.2 Tri-Phasic A/D Converting

The A/D converter as described in paragraph 4.1, integrates the conditioned input signal during Phase 2 and the appropriate reference voltage in Phase 3. In both of these phases an offset for internal drifts, determined during the autozeroing phase, Phase 1, is algebraically combined with the input voltages. The function of the A/D is to produce a timing pulse at the end of conversion that determines the duration of Phase 3. This interval (Phase 3) gates the counter in the digital logic in order to accumulate the digitizing count.

The circuit configuration for each of the three phases in the A/D conversion is established by switches labeled A through F in Figure 4-1, and controlled by signal levels P1, P2, P3+, and P3−, from the digital logic programmer block. During the autozero phase, level P1 closes switches B, C and F. Switch F closes the loop around the converter and charges capacitor CB until it offsets any non-zero effects in the loop. Switch C controls the voltage developed on capacitor CA. If not in −60/−20 dBm measurement function, then capacitor CA is effectively shorted by switches B and C. If measuring dBm, then CA is charged to the offset value 0.04V in −20/−60dBm.

During Phase 2, level P2 closes switch A, connecting the conditioned input in series with the voltages on capacitors CA and CB as input to the A/D converter for exactly 100 milliseconds. During this time the integrating capacitor in the A/D is charged at a rate proportional to the voltage at its input. At the end of Phase 2, the logic senses the output of the integrator and determines the polarity of the reference voltage to be applied during Phase 3. If a positive input has been applied, control level P3+ is generated, closing switch E, and connecting a negative reference to the A/D during Phase 3. Switch D is closed by control level P3− if a negative input signal is sensed. Phase 3 and level P3+ or P3− remain effective until the logic senses the end of conversion and control level P1 is generated to start the autozeroing phase and the next conversion cycle.

If the conditioned input exceeds 200 millivolts, the digital logic will not sense an end of conversion within 2000 counts and will generate control level FC and the out-of-range control BNK. The FC signal is used in the A/D converter in order to quickly reduce the remaining voltage at the integrator output to zero so that there will be no residual effect of a prior conversion in the digitizing action of succeeding ones.

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4.2.3 Digital Logic Programming

This functional block, including the master oscillator, develops the conversion cycle timing control signals as described above, generates the BCD signals from its counter output, the polarity control signal for the display, and when appropriate, the blanking control signal for out-of-range inputs. The BCD output is multiplexed on four parallel lines in synchronism with a digit-indicating level on the address lines.

4.2.4 Decoder Driving

This block translates the four BCD signals for each digit into the appropriate group of drivers for up to 7 segments to be lit in the display for that digit. The out-of-range signal from the programmer is also used in this block to develop the digit blanking indication in the display.

4.2.5 Displaying

The display function is instrumented in four LED digits, the most significant digit (MSB) displays the polarity and a "1" and or a decimal point, as appropriate. Each of the three remaining digits are full decades and a decimal point. The MSD is driven directly from the logic, while each of the other digit's data values are enabled by the digit scan in synch with the segment drives.The decimal point is driven by a control signal generated by the range switch.

4.2.6 Power Supplying

This block includes a charger circuit which develops raw dc for a battery pack (if installed) and input to the DC DC converter. The converter supplies the analog power of - 6.8V and + 7.5V and references of 0.1V and 0.04V; the - 6.8V is also used to power the digital logic circuits. The battery voltage is sensed and when it drops below a preset threshold, the sensing circuit causes the decimal point to blink.

4.2.7 Timing Diagram

Figure 4-2A summarizes the time relationship among the phases and the waveform at the integrator output for an in-range signal. Figure 4-2B illustrates the effect of an out-of-range signal on the timing.

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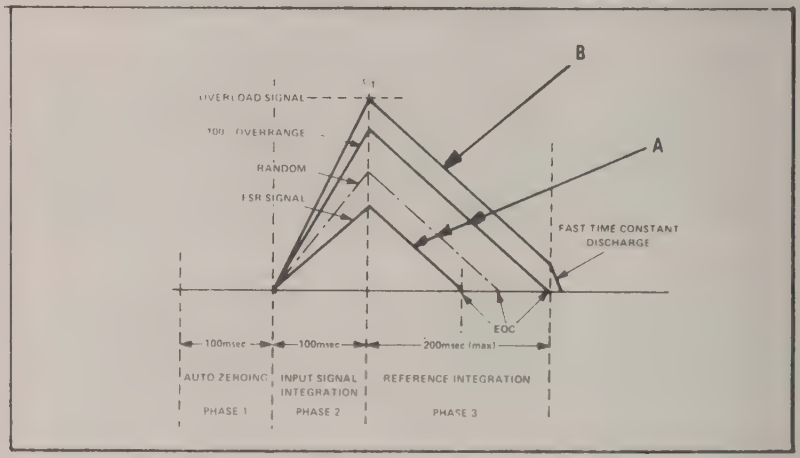

Figure 4-2. System Timing Waveforms

4.3 INPUT SIGNAL CONDITIONING DETAILS

4.3.1 General Requirements

a. As described in paragraph 4.2, the signal conditioning function converts the input parameter of voltage, current, resistance or dBm (relative magnitude) into a dc voltage scaled for 100μV per count in Phase 2 of A/D operation. The scaling may be accomplished in the input attenuator, in the RMS or dBm converter, and/or at the input to the A/D circuit. Table 4-1 summarizes the scaling factors introduced for the selected range scales in each measuring function so that the input to the A/D integrator will be 100mV for nominal full scale (1000 counts).

b. Note the use of a gain of 10 at the input to the ac to dc converter. This action introduces a higher signal level for more reliable and accurate operation in the converter. Note also that the converter output is attenuated by 10 for ac measurements to obtain the desired sensitivity at the input to the A/D, while the dBm output is divided by 3 to account for the scaling within the converter.

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4.3.2 DCV Scaling

The attenuation is accomplished by a resistor divider network, as shown schematically in Figure 4-3 for a selected range of 1. As shown in the schematic, the network is switched across the input by the activation of switches marked "DCV" and the non-activation of switches marked K9(Hi) and K9(Lo). The range selection switching has been greatly simplified for this sketch, and for the others in this chapter.

4.3.3 DCmA Scaling

Figure 4-4 illustrates the shunt and attenuation operation when measuring dc currents on Range 1. Note the 2A fuse in series with the input, and the clamping action of CR3, CR4, CR5 and CR6. These protect the DMM circuitry from excessive currents and limit the maximum voltage to the A/D input to approximately ±2 volts. The network is switched into the circuit by closing the switches activated by "DCmA".

Table 4-1

FRONT PANEL		MODEL 1750 DMM SCALING OPERATIONS					
Selected Function	Selected Range	Input Attenuation or Standard Resistance (kΩ Measurement)	RMS or dBm Converter			DC Ref Voltage for Phase 3	A/D Input Amp
			Input Amp	Converter	Output Ckt		
DCV DCmA	100mV μA 1V mA 10V μA 100V mA 1000V mA 10A	1:1 1:10 1:100 1:1000 1:10000 1:1				0.1V	10:1
ACV ACmA	100mV μA 1V mA 10V mA 100V mA 1000V mA 10A	1:1 1:10 1:100 1:1000 1:10000	10:1	Avg/rms	1:10	0.1V	10:1
Ω 2W 200mA	100Ω 1kΩ 10kΩ 100kΩ 1MΩ 10MΩ	100Ω 1kΩ 10kΩ 100kΩ 1MΩ 10MΩ				See Para 4.2.1	10:1
Ω HV 2W	1kΩ 10kΩ 100kΩ 1MΩ 10MΩ	1kΩ 10kΩ 100kΩ 1MΩ 10MΩ				See Para 4.2.1	1:1
dBm 600Ω	Not Used	1:1	10:1	1mV = 1dB	1:3	2.19V	10:1
dBm 2MΩ	Not Used	1:100	10:1	10mV = 1dB	1:3	2.19V	10:1

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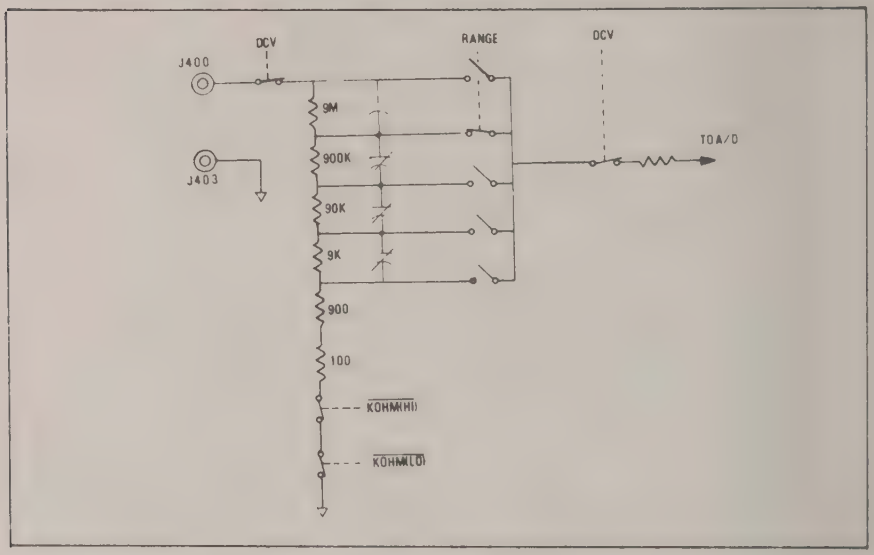

Figure 4-3. DCV Signal conditioning schematic

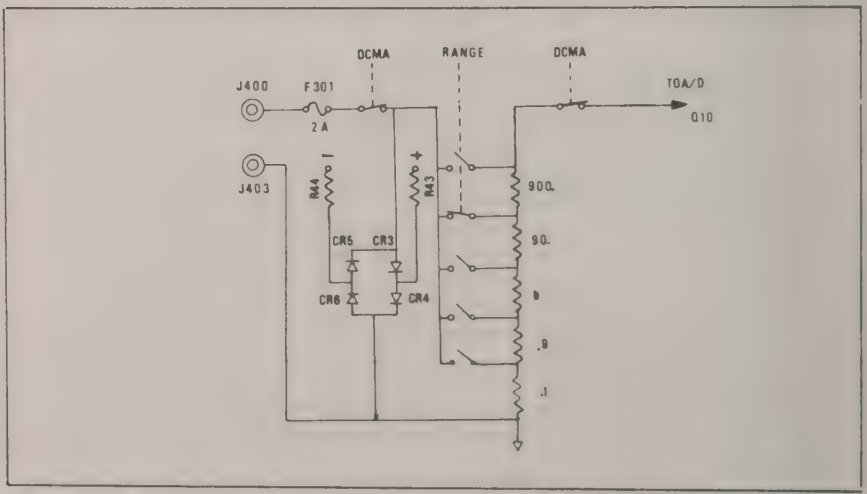

Figure 4-4. DCmA Signal conditioning schematic

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4.3.4 ACV Scaling and True RMS Conversion

a. As shown in Figure 4-5, the ac voltage input is first scaled in the same divider network as used in the dc voltage conditioning. The frequency-compensating components shown in Figure 4-3 (which are not effective for dc voltages) are used to correct for impedance mismatches.

b. The attenuated ac voltage is direct-coupled to Z2, a gain of 10 amplifier, whose output is capacitively coupled to the ac-to-dc converter Z3. Z3 is a dual function component, as configured by the switching at terminals 7, 5, and 8. When terminal 7 is jumpered to 8, the output at terminal 6 is the True RMS conversion of the input value. That output is attenuated by the resistor string R24, R25 and R26 and the output switched to the A/D input.

c. Potentiometer R22 adjusts the zero of Z3, and R25 adjusts the gain of Z3.

4.3.5 ACmA Conversion, Scaling and True RMS Conversion

The conditioning of ac currents utilizes circuitry already discussed. The input is fused, limited, attenuated, amplified in Z2, and then converted in Z3 to a dc voltage equal to the True RMS of the scaled value.

4.3.6 Kilohms Current Sourcing

a. Model 1750 provides 2 sourcing levels, one at 200mV (approximately) and one at 2V (approximately). These drives are generated in a circuit illustrated in simplified schematic form in Figure 4-6. A reference voltage is derived from the + 7.35V filtered supply. When in KΩ(Lo) measuring function, the output of Z1B is regulated by the servo loop containing Z1B and pass transistors Q1, Q2 and Q3, and the output driving the standard and unknown resistance in series is about 200mV, as required.

b. When in KΩ(Hi) the inverting input to Z1B is grounded, causing the output to go to saturation. The saturated output, limited by pass transistors Q1, Q2 and Q3 and diode CR1, develops a nominal 2V to drive the resistance load. The switch that causes the 2V output configuration in the voltage source also controls the gain of the input amplifier to the A/D converter. Thus, a 10X higher voltage source is compensated later in the chain.

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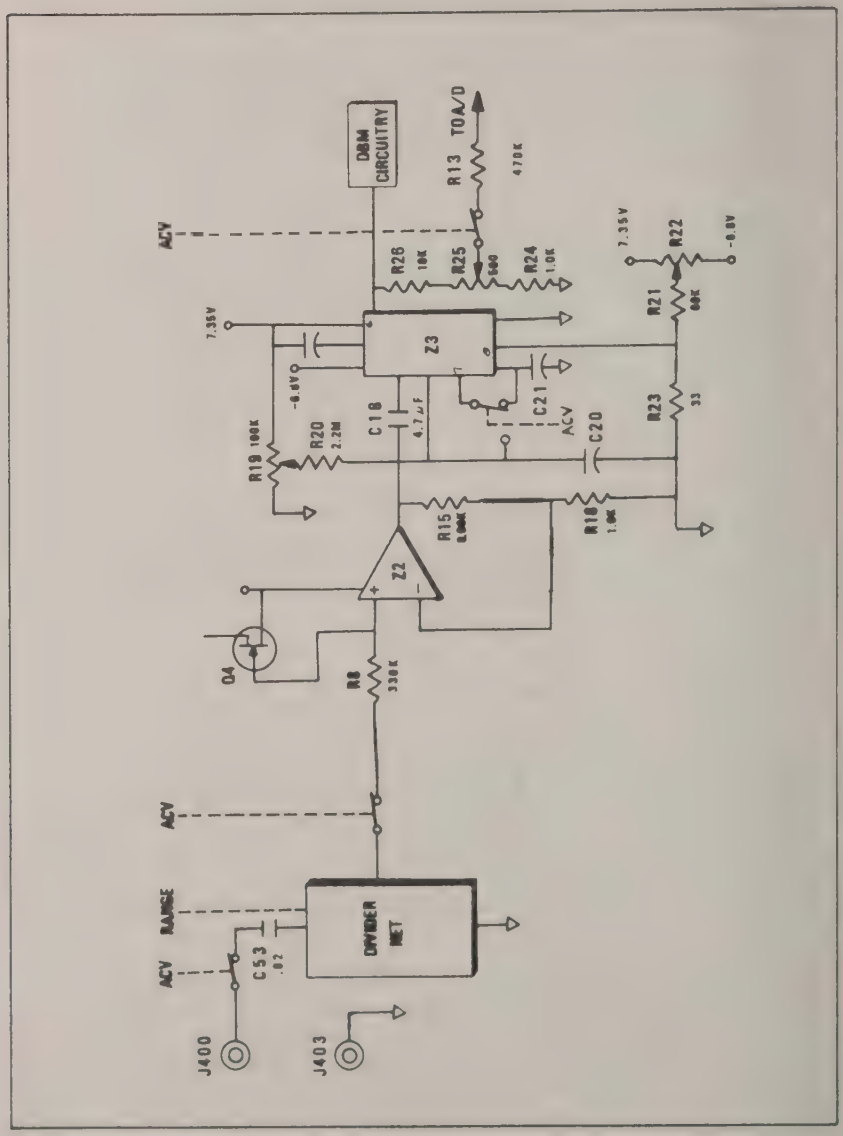

Figure 4-5. ACV Signal conditioning

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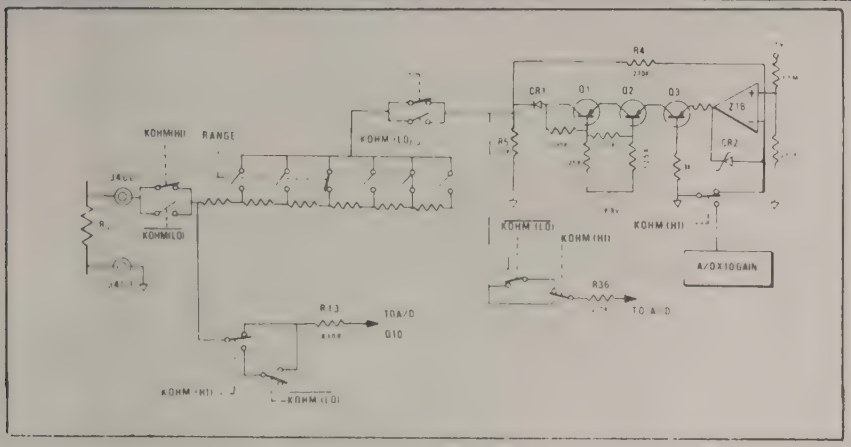

Figure 4-6. Voltage source generation for resistance measurements

c. Figure 4-7 illustrates the Ratiohmic operation of the Model 1750 when measuring resistance. During Phase 1 (autozero) the closing of Q13 charges C25 to the value of the ohms excitation voltage appearing across standard resistance R_s and load resistance R_x in series. (Let this be $V_s + V_x$.) During Phase 2, switch Q10 connects V_x to the A/D input. During Phase 3, switch Q14 connects the high side of the capacitor C25 to the level of V_x and the low side of C25 will then be $V_x - (V_s + V_x) = -V_s$. In other words, this generates a reference voltage of opposite polarity to the input and a magnitude proportional to the range-selected standard resistance. The A/D digitizes the ratio of these two. Hence, the term Ratiohmic.

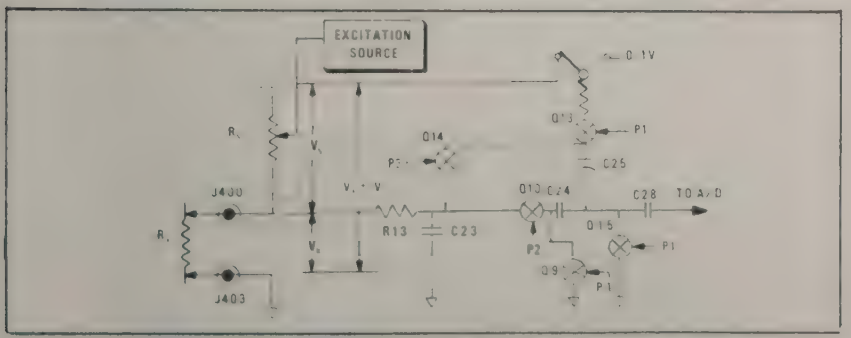

Figure 4-7. Ratiohmic measurement

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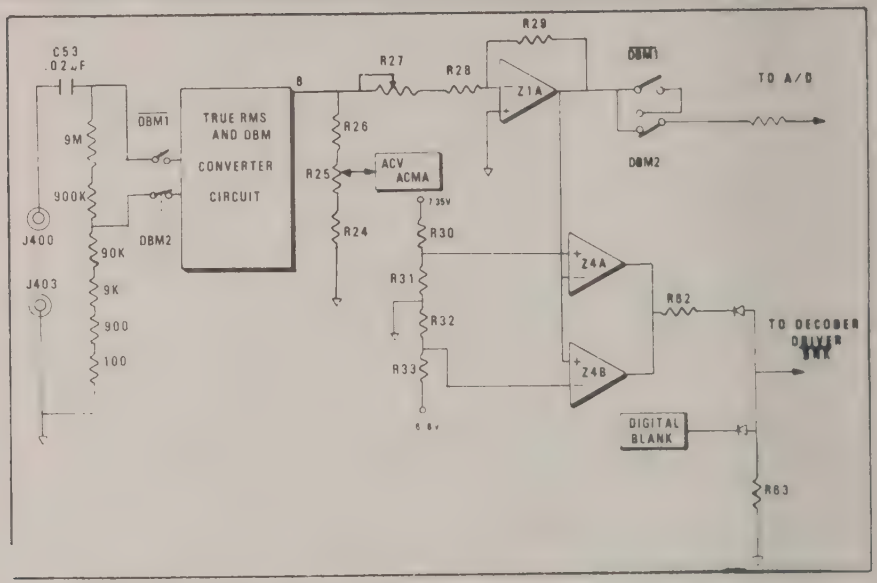

Figure 4-8. Conditioning for dBm measurements

4.3.7 dBm Signal Conditioning

a. As shown in Figure 4-8, pushbutton selection of the dBm measuring function in the range -20 to +20 connects the input through a 100:1 setup of the input attenuator, while selection of the -60 to -20 function pushbutton inserts a 1:1 attenuation of the input. The 100:1 attenuation offsets the input by 40dB, and the attenuator outputs for either input are at the same sensitivity (dBm per volt). (A compensating offset of 40 millivolts is introduced later in the A/D function to obtain a correct value for the −60 to −20 function selection.)

b. The scaled output of the attenuator is connected to Z3, where it is transformed to a voltage output at Pin 6 at a sensitivity of 3mV per dB. Then, as shown in Figure 4-8, that value is scaled in the operational amplifier Z1A so that it is connected to the A D converter at the standard sensitivity of 100 microvolt per count.

c. An out-of-range signal for the dBm function is developed for values that are approximately 5dB outside the selected range. This is accomplished at the analog signal conditioning as shown in Figure 4-8 by the

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comparators Z4A and Z4B. The dBm output of Z1A is compared with references of ±30mV, respectively. When Z1A output exceeds 30mV magnitude, a display blanking signal is transmitted to the standard control function.

4.3.8 10A Signal Conditioning

As shown in the system schematic in Chapter 6, the 10A input at connectors J401 and J402 is shunted by R400 = 0.01Ω, developing a voltage of 100 millivolts for the full scale 10A input.

Thereafter, the signal conditioning and digitization is the same as for other current input signals.

4.4 TRI-PHASIC A/D CONVERTER DETAILS

Figure 4-9 is a schematic of the analog portion of the circuitry accomplishing the A/D conversion. It contains a programmable gain noninverting amplifier Z7, integrating amplifier Z8A comparator Z8B, FET switches Q9 through Q17, and associated passive components.

4.4.1 Phase 1 Operation (Autozeroing the A/D)

a. Operation of the tri-phasic A D converter is determined by the switches that are set by control levels P1, P2 and P3, for phases 1, 2 and 3 respectively. During Phase 1, switches Q16, Q9, Q15 and Q13 are closed, all others remain open. Q16 closes the loop around Z7, Z8A and Z8B, connecting the comparator output to the input, while Q15 grounds any other input. Any non-zero signals within the active elements of the loop develop a voltage across capacitor C28 until the comparator output is driven to -3.4V. The C28 voltage is stored for use in later phases to compensate for these non-zero signals as the autozeroing action in each conversion cycle.

b. Also during Phase 1, switch Q13 connects the 0.1V reference voltage across C25 to charge that capacitor to the 100 millivolt reference value. In addition, switch Q9 causes capacitor C24 to be charged to the 40mV value if in 60 20 dBm mode, or to zero value for other modes.

4.4.2 Phase 2 Operation (Integrating the Conditioned Input)

a. During Phase 2, switch Q10 connects the conditioned input in series with the voltage offsets on capacitors C24 and C28 as input to the A D

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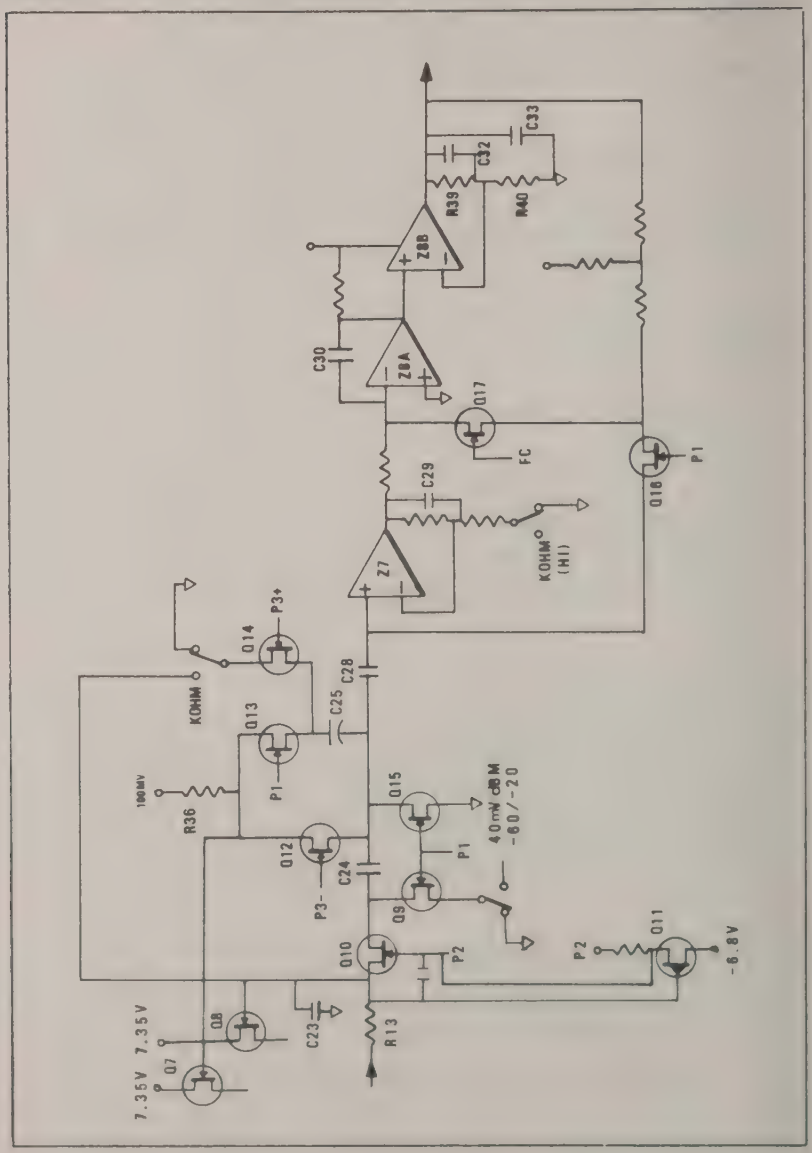

Figure 4-9. A/D Converter schematic

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Amplifier Z7 is configured as a gain of 10 for all functions other than kΩ(Hi) and for unity gain for kΩ(Hi) to compensate for the 10 times greater excitation voltage in that mode. See paragraph 4.3.6.

b. Phase 2 lasts for exactly 100 milliseconds, as determined by the digital logic programmer, during which time the integrator charges capacitor C30 at a rate proportional to the output of Z7.

4.4.3 Phase 3 Operation (Integrating the Reference)

a. At the end of Phase 2, the comparator output is sensed to determine the polarity of the conditioned input. (The high gain comparator is driven to saturation in the opposite polarity to the input.) The logic circuitry develops a P3+ control level for positive input signals, or a P3− control level for negative input signals. P3+ closes switch Q14 to connect the high side of C25 to ground for other than kΩ functions. (See paragraph 4.3.6 for A/D operation in kΩ function.) When the high side of C25 is grounded, the low side is then negative 100mV. P3− closes switch Q12 to connect the +100mV reference to the A/D input. During Phase 3, the integrator reduces the voltage on C30 at a constant rate for the 100mV magnitude until the output of Z8A crosses zero, and the comparator Z8B is driven toward saturation in the opposite polarity. The change in Z8B output is sensed as the End of Conversion (EOC) and the logic programmer ends Phase 3 and initiates Phase 1 to start the next conversion cycle.

b. If the comparator output does not change polarity within 2000 counts, the logic programmer develops out-of-range and FC control signals. The FC signal closes Q17 to connect the comparator output to the integrator. This action applies a high level signal of proper polarity to drive any remaining charge in C30 quickly to zero so that no residual voltage remains on C30 during the autozeroing phase.

4.4.4 Iso-Polar Reference Generation

Figure 4-9 and the previous explanation illustrates the patented technique of iso-polar reference generation. It should be noted that both positive and negative reference voltages are *exactly* the same magnitude and that the polarity is determined solely by the switching action controlled by P3+ or P3−. This design eliminates any unbalance that may be introduced by generating positive and negative references by separate components, designed to be equal, but nevertheless made unequal by uncontrollable environmental effects and noise.

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4.5 MASTER OSCILLATOR & DIGITAL PROGRAMMER

a. The digital logic programmer circuitry is contained entirely on one CMOS solid state component, Z9. As shown in Figure 4-10, it contains:

4 Decade Counter and the MSD flip-flop
Latching BCD Output Register
Clock Generator
A/D Phase Signal Generator and Fast Charge Control
Polarity and Overload Detection Logic

b. In addition to the phase control signals described earlier, digital logic chip Z9 outputs the latched register BCD values series-by-digit, parallel-by-bit on 4 BCD output lines. The digit address for 4 decades of BCD data is indicated as a high level on four lines. Only 3 full decades are used in Model 1750, but the fourth (least decade) is also used when the BCD option is installed. Separate output lines indicate the binary value of the MSD (0 or 1), and the polarity (binary + or −). The binary overload condition is also indicated on a separate Z9 output line, $\overline{BNK}$.

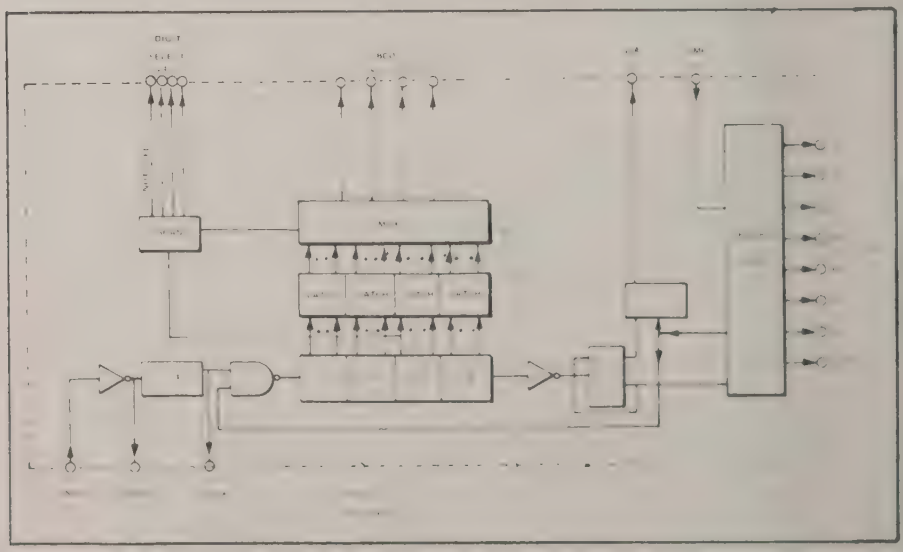

Figure 4-10. Digital logic programmer schematic

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c. The master clock oscillator circuit containing resonator Y1 oscillates at 400kHz. This frequency is counted down by 4 in Z9 to obtain a basic counting rate of 100kHz so that the carry from the 4-decade counter represents an interval of 100 milliseconds for Phase 1 and Phase 2 timing. An MSB divide-by-two flip-flop at the output of the 4-decade counter is used to sense the MSB of 10^4 counts, and, when digitizing an overload input to the A/D, senses $2 \cdot 10^4$, from which the $\overline{BNK}$ blanking control and FC fast discharge control signals are developed.

d. Figure 4-11 is a summary of the timing relationships of the waveforms generated in Z9. Conditions when converting an in-range A/D positive input are shown in the upper portion and for an overload negative input in the lower portion of the illustration.

4.6 DECODER DRIVER & DISPLAY DETAILS

a. Decoder-driver Z10 converts the multiplexed 4-bit BCD outputs from Z9 into 7-segment format. The 7-segment control signals are connected in parallel to all 3 digits, DS102, DS103 and DS104 of the display, while the address lines D4, D3 and D2 control which of the display digits is enabled. In effect, the digit address selects the display digit that responds to the 7-segment drivers. Address line D1 (the least significant decade in Z9) is not used for the $3\frac{1}{2}$ digit display, but is used as a control signal to the BCD option, when installed. The most significant digit in Model 1750, DS101, is driven by the MSB output signal through driver Q20. Address signals D4, D3, and D2 enable display digits DS102, DS103 and DS104 through drivers Q21, Q22 and Q23, respectively.

b. The display is assembled on a separate flexible PC. It contains the four display digits, including sign and decimal points. Current limiting resistors for the segment drivers of the three full decades, transistor driver circuits for the most significant "1" (when appropriate), and for the polarity (plus or minus) are located on the main circuit card. Range-selected control signals drive the decimal point in the appropriate decade through current limiting resistors.

4.7 DC/DC CONVERTER & POWER SUPPLY

a. Z5 is a linear switching regulator driven by the CLK output of Z9 at 100kHz. Internal action of Z5 keeps current from the battery (or battery charger) flowing in one direction through inductance L1 to generate a regulated output at Z5, Pin 6.

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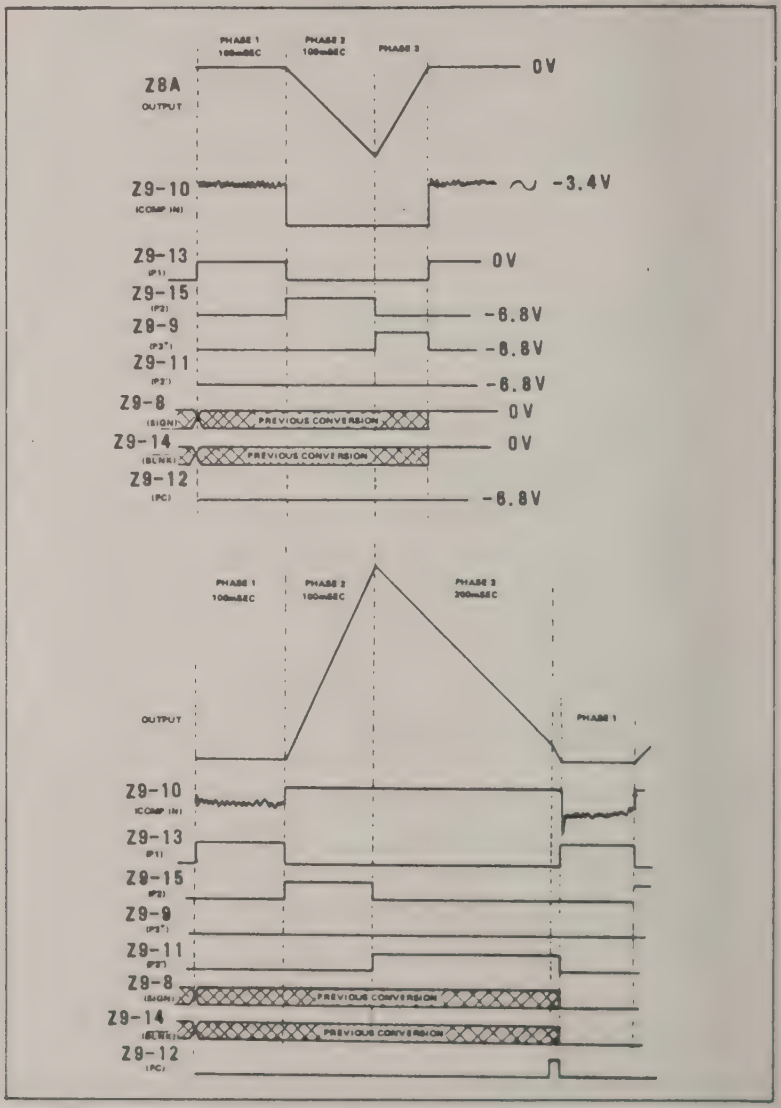

Figure 4-11. Digital programmer timing waveforms

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b. Amplifier Z6A and reference zener CR9 are connected in a voltage regulator circuit that results in a regulated +7.35V with respect to COM. Voltage divider networks R55, R56, R57, R58, R59 and R60 are used to develop the +0.1V reference levels for the Phase 3 A/D integration and the +0.04V offset for the dBm −60 −20 conversion. R53 and R59 are the calibrating adjustments for these voltages, respectively.

c. Amplifier Z6B is connected as a comparator in which the battery voltage is compared with the 0.1V reference and the output drives Q18. Transistor Q18 is gated by the output of Z6B when the battery voltage drops to 6.9 volts, and is turned on and off by the Phase 1 waveform, providing a blinking signal for the decimal point at a $2^1/_2$ per second rate, corresponding to the conversion rate.

4.8 BCD OUTPUT OPTION

a. The isolated BCD ouput option provides isolated digital outputs of data and status signals for remote application of the Model 1750 DMM. The option is instrumented in a flex-print assembly, as shown in Figure 4-12, and the printed-circuit edge connectors mate with receptacles mounted on the main PC-card assembly (Figure 5-2). The assymetrical connector assemblies assure proper alignment of mating connectors.

b. Figure 4-13 is a schematic of the BCD Output Option circuitry. In brief, as shown in that illustration, the 4-wire BCD outputs of the converter are opto-isolated, and the isolated BCD values are de-multiplexed by opto-isolated digit address signals. Range-select signals are independently isolated, while status signals (OVLD, SIGN, MSB) are time shared with the "1," "2," "4," and "8" BCD values of the three less significant digits prior to the isolation of both groups.

The Phase 1 timing signal, P1, from the A/D converter is used to program the BCD output operation. When the P1 signal goes low, signifying the end of phase 1, the BCD inputs to the card are connected through the opto-isolators. This timing provides assurance that the data values on the BCD lines are stable after the previous conversion. (P1 gives low at least 100 milliseconds after the end of conversion.) The isolator outputs are connected to latching registers that are enabled by opto-isolated address lines derived from D2, D3, D4, and D1, respectively.

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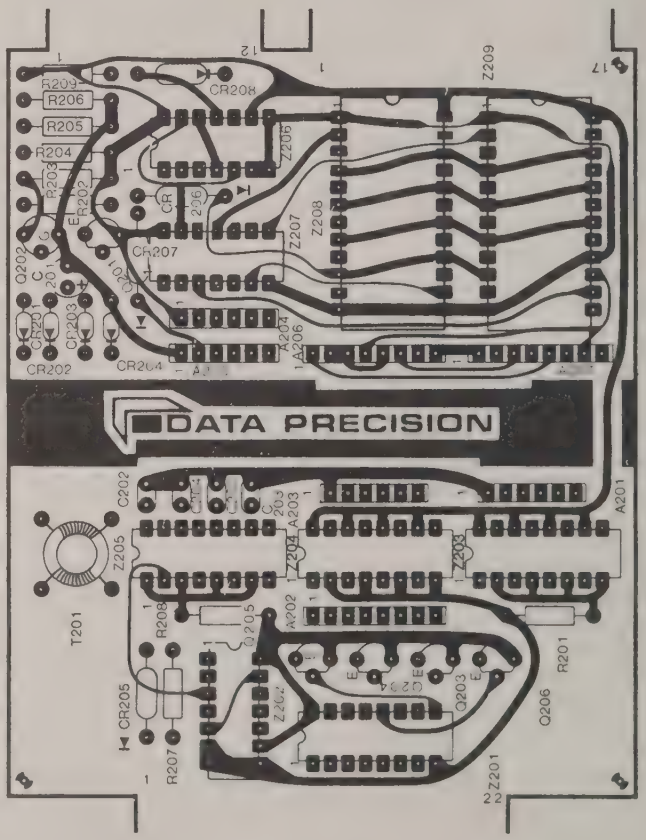

Figure 4-12. Isolated BCD Output (option) assembly drawing

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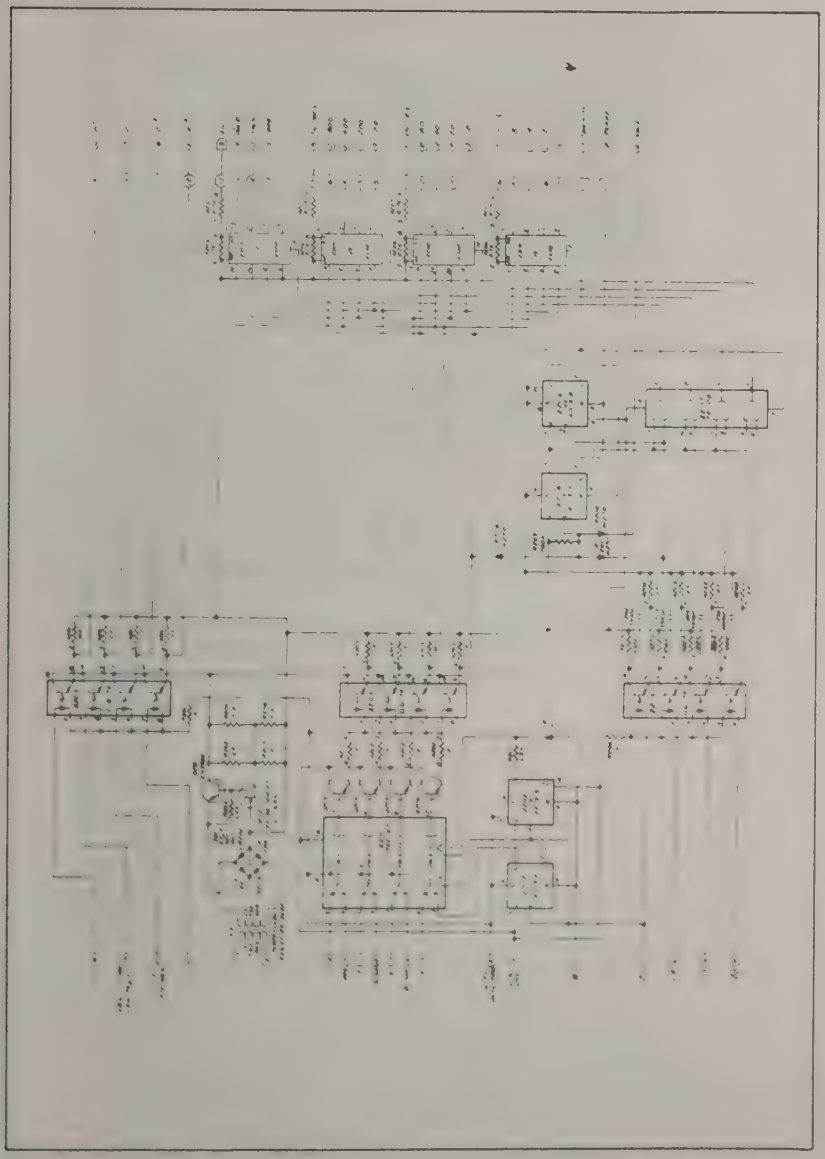

Figure 4-13. Isolated BCD Output (option) schematic drawing

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c. The BCD outputs include a READY signal that is derived from the timing sequence. The READY line (pin 18) remains low during the demultiplexing sequence, and indicates that the data lines are being updated during that interval.

d. A digital control signal, $\overline{\text{HOLD}}$, is available to the user at terminal 14 of the BCD connector. When that terminal is held at logic zero (low level), latching registers can not be updated, and retain the previously transferred data.

4.9 BRIGHT DISPLAY OPTION

a. The bright LED display option is mounted on a flex print assembly that is interchangeable with the standard assembly (Figure 5-2) Schematically, the circuits appear identical; the bright display utilizes high efficiency emitter components.

b. To replace the display assembly in the field:

(1) Remove the four retaining caps (one at each corner of the display) (Figure 4-13).

(2) Unplug the pc-card edge connector.

(3) Reverse steps (1) and (2) when inserting the new assembly.

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Chapter 5

MAINTENANCE

5.1 GENERAL

CAUTION

The Model 1750 Multimeter is covered by a one-year warranty and should be referred to the factory for maintenance within the warranty period. Attempts to make any extensive repairs within the warranty period may invalidate the warranty. If repairs are needed after the warranty period, only qualified technicians should attempt to effect such repairs and should use test instruments and standards calibrated within the accuracy and tolerances of the specifications.

5.2 TROUBLE-SHOOTING FLOW CHART

Should the meter performance indicate a possible need for repair, a well-defined strategy should be used to isolate the cause of trouble. This is illustrated in Figure 5-1. It indicates a sequence of steps in terms of standard symbols and defines a program of actions based on a philosophy of positive maintenance. The positive approach isolates to the faulty sections by verifying proper operation of the remaining instrument section.

5.3 TEST POINTS

The test sequences identified in the chart of Figure 5-1 are described in step-by-step detail in the paragraphs that follow. In performing the tests detailed in these paragraphs, the maintenance technician is directed to make measurements at designated test points which have been placed at significant portions in the circuit. The special test points are identified by E-reference numbers, and their locations on the printed circuit board are shown in Figure 5-2. Other test points designated in the test procedure paragraphs may be pin terminals of circuit components, and technicians should refer to component data sheets for the pin terminal locations as well as to Figure 5-2. Use caution in attaching test leads to avoid accidental shorting of adjacent components. The use of EZ Mini Hook®, or equivalent is suggested to aid in making good connections

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5.4 CLOSED-METER TESTS (FIELD MAINTENANCE) TS5-1

a. The first test sequence is performed with the "cased" meter. The sequence is fully detailed in the illustration of Figure 5-3.

b. Model 1750 DMM may exhibit certain battery performance below rated characteristics that are only temporary operation effects typical of battery usage patterns. Such below-specification performance can be corrected easily and in a minimum of time. See Chapter 2, Paragraph 2.5.1.

c. Maintenance of a "closed-case" meter is limited to the replacement of battery pack or fuses (although battery pack assembly replacement requires removal of cover, it does not affect internal components). However, a number of malfunctions may be diagnosed in a closed-case condition. If the Model 1750 DMM makes apparently accurate voltage and resistance measurements, but current measurements are apparently nonoperative, then Fuse F301 (see Figure 2-3) should be checked, and replaced if open. If the fuse replacement does not remove the malfunction, then the shunt circuit is suspect, and should be checked after obtaining access to the assembly. Refer to Paragraph 5.5. If there appears to be no meter response at all (refer to Chapter 2), and the power source is satisfactory, check the line fuse, F300 (see Figure 2-3).

d. Among the closed-case symptoms that may be trouble-shot are the following:

(1) If the same segment in each digit malfunctions, then the faulty component may likely be the decoder/driver, Z10 or a ballast resistor in A6 or A7.

(2) If one digit only is completely blank, then the faulty component may be the digit address geneator, Z9, or the respective transistor switch enabling power to that digit, (Q21, Q22, Q23).

(3) If either dc voltage or current measurements are apparently correct, but not both, then the faulty component(s) may be either the current shunt(s), or the voltage divider networks or fuse, F301.

(4) If dc measurements are apparently accurate, while ac measurements only appear to be in error, then the faulty circuitry may likely be the AC/DC converter, including Z3.

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e. To check the battery, disconnect the ac line source. If that action changes an apparent accurate measurement to an inaccurate one, and a full recharging cycle does not restore the accurate measurement, then the battery assembly should be replaced.

5.5 OPEN-METER TEST/MAINTENANCE

5.5.1 General

a. If the multimeter does not perform correctly after the tests of TS5-1 are satisfactorily completed, then it is likely that repairs to an internal assembly are required. The sequence of such tests is indicated in the overall strategy of Figure 5-1, and is identified by a TS number for further reference. Each test sequence paragraph includes the designation of test points, the indications of proper performance, the circuits that are checked when proper performance is observed, and the circuits that should be examined in greater detail when indications of improper performance are recorded. Refer to the fold-out schematic in the back of this manual for complete circuit details, and to Chapter 6 for replacement parts identification.

b. Some of the troubleshooting hints of Paragraph 5.4 lead to repair replacement of internal components. These repair activities may be accomplished prior to performing any of the actions that are described in the paragraphs that follow.

5.5.2 Access to Main and Display Assembly

Remove the two (2) screws fastening the top cover to the rear panel (Figure 2-2). Lift up the cover and remove it, thereby obtaining access to all main assembly components. See Figure 5-2. The display assembly is connected to the main board via a flexible flat-cable and is fastened to the front panel at four corner posts by flexible caps. (See Figure 5-2.)

5.6 TEST EQUIPMENT

Test instruments and reference standards needed for the trouble shooting analysis should have the following characteristics

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PARAMETER	RANGE	ACCURACY	MEASURE/ GENERATE* M/G
DC Voltage	−10V to +10V	±0.1%	M/G
AC Voltage	1kHz 100mV 10kHz 200VRMS 100VRMS 10VRMS 1VRMS	±0.1%	M/G
Timing Waveforms	Oscilloscope 5MHz BW	± 5%	M
Resistance	0 to 10MΩ	±0.1%	M/G

* Measure = indicates test instrument. Generate = indicates source instrument.

5.7 POWER SUPPLY TEST TS5-2

a. Select KΩ Mode and 10MΩ Range positions. Turn power ON.

b. Check for the indicated dc voltages at the test points shown below and adjust as shown in Figure 5-4.

Test Points*	Measure Value*
E7	−6.8V ±0.2V
E8	+7.35V ±0.15V

*Measurements are made with respect to E2.

c. If all readings are correct the DC/DC converter and regulator are operating satisfactorily. An incorrect reading may result from a short circuit in one of the components driven by the power supply or by a failure within the DC/DC converter.

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5.8 DIGITAL LOGIC TS5-3

All the digital logic functions are essentially implemented in two CMOS chips, Z9 and Z10. The separate and sometimes independent functions performed by these LSI circuits are checked as shown in Figure 5.5. Proceed as shown below. (A simplified block diagram of Z-9 is shown in Figure 4-10.)

5.8.1 Time-Base Generation

Check 100kHz Clock. Waveform at Z9-23 should have 5.5V p-p amplitude. If not, trace from origin at master timing oscillator and Z9.

5.8.2 Program Logic

a. Connect Z9-10 to Z9-5. Simulates overload input.

b. Observe waveforms at Z9 outputs and compare with those illustrated in Figure 5-7. If satisfactory, then Z9 is functioning properly.

5.8.3 Decoder/Driver Logic

a. Observe display. If indication is of an overload input (blanked digits), then Z10 function is partially checked.

b. Short Z10-4 to ground (Z10-3) and connect Z10-7, Z10-1, Z10-2, Z10-6 to Z10-5. This action simulates a zero value out of the counter of Z9.

c. Observe display. If indication is 000, Z10 is functioning properly.

d. Remove all shorting jumpers.

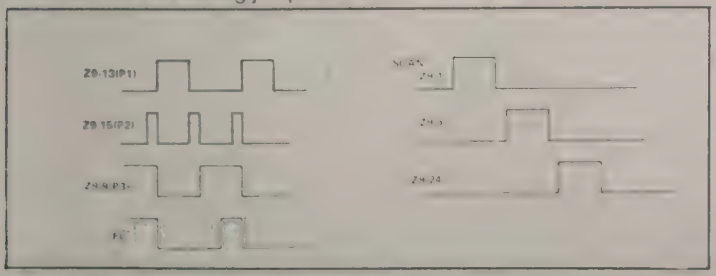

Figure 5-7. Program Logic Waveforms

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5.9 A/D CONVERTER & SIGNAL CONDITIONERS TS5-4

5.9.1 Analog A/D

a. Select DCV measuring function.

b. Connect Z9-13 to ground, E2, and Z9-9, Z9-11, Z9-12, and Z9-15 to Z9-5 (-6.8V). This places the A/D in Phase 1 auto zero operation.

c. Observe output of comparator Z8-1. Proper functioning of the auto-zero loop is indicated by the appearance of noise of about nominal IV amplitude. If output (Z8-1) is saturated (high or low) then check Z8.

d. Signal trace through A/D by following the steps shown in Figure 5-6. Remove shorting connections when finished.

5.9.2 AC/DC Signal Conditioner

a. Select ACV function. Range 100mV.

b. Apply 100mVRMS sinusoid @ 1kHz to J400 and J403.

c. Observe waveform at Z2-6. A sinewave of approximately 2.73V peak-to-peak amplitude at 1kHz indicates proper operation of scaling amplifier Z2.

d. Observe dc level at Z3-6. A dc level of approximately 0.966VDC indicates proper operation of TRUE RMS converter, Z3.

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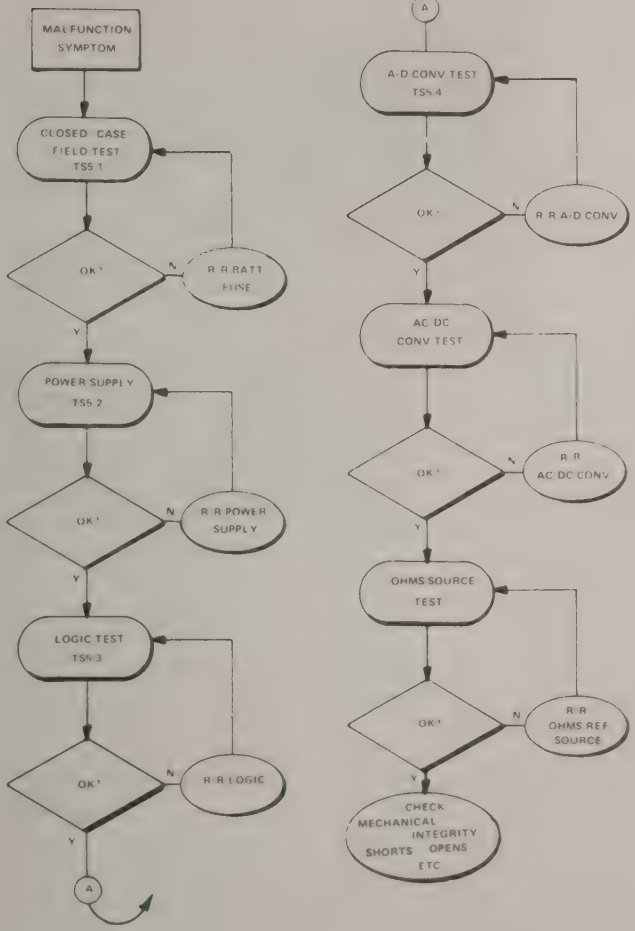

Figure 5-1. Trouble Shooting Flow Chart

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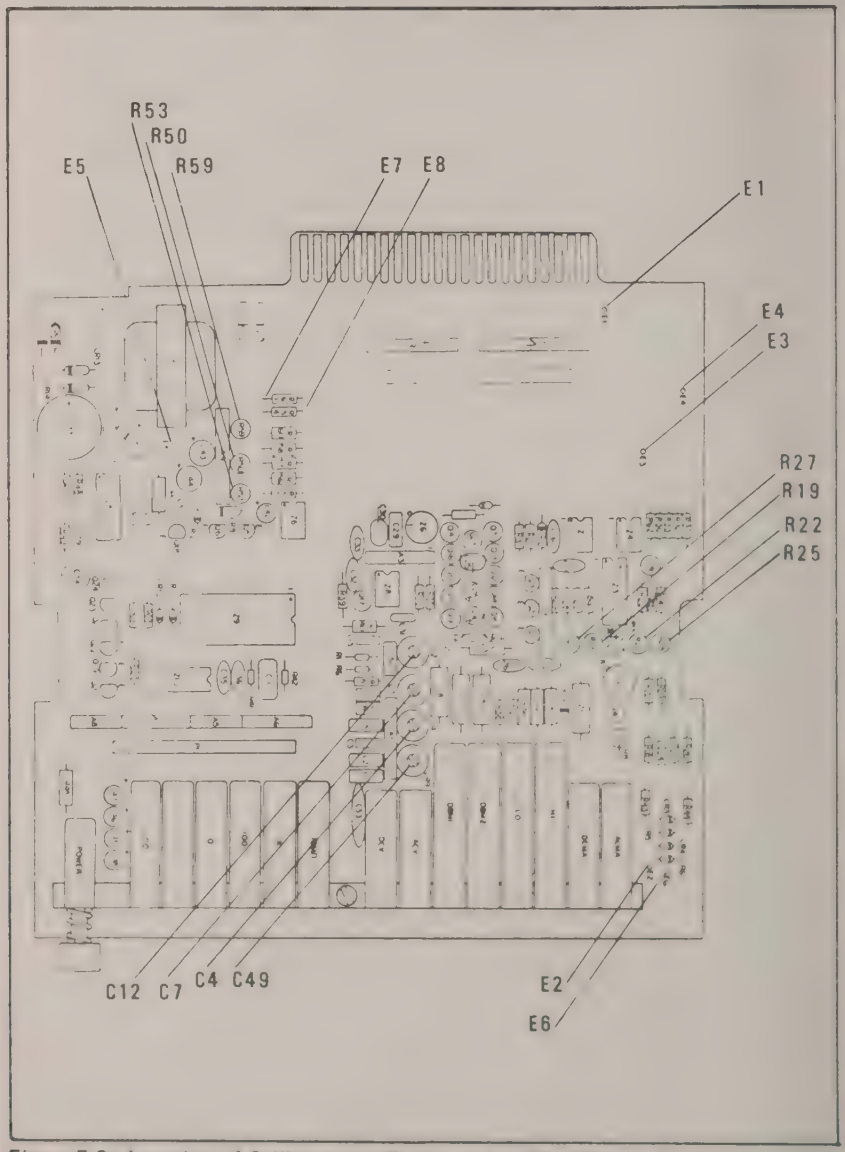

Figure 5-2. Location of Calibration Adjustments and Test Points

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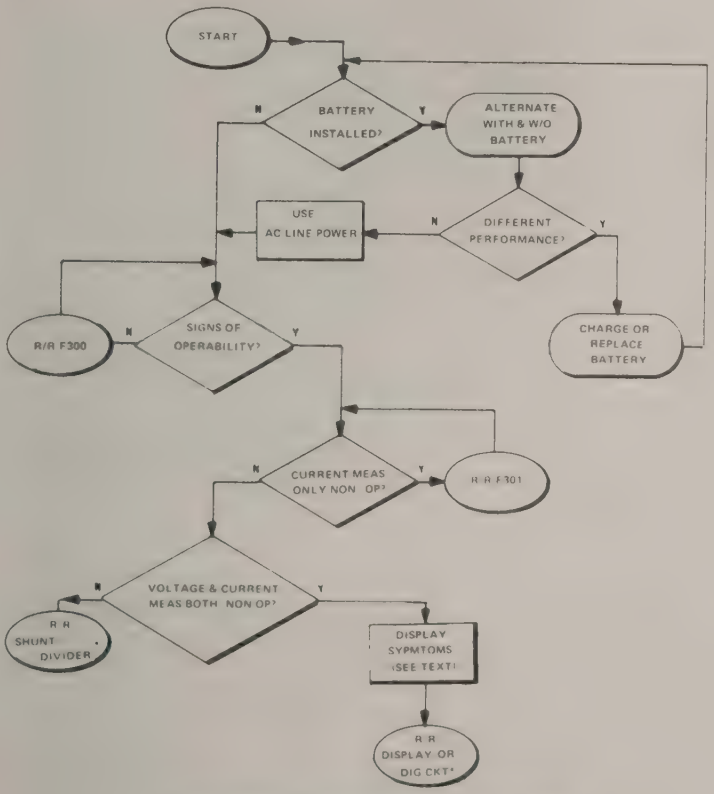

*TO BE PERFORMED AFTER OPENING CASE FOR CIRCUIT REPAIRS REFER TO PARAGRAPH 5 5 1b

Figure 5-3. Test TS5-1, Closed Case Trouble Shooting

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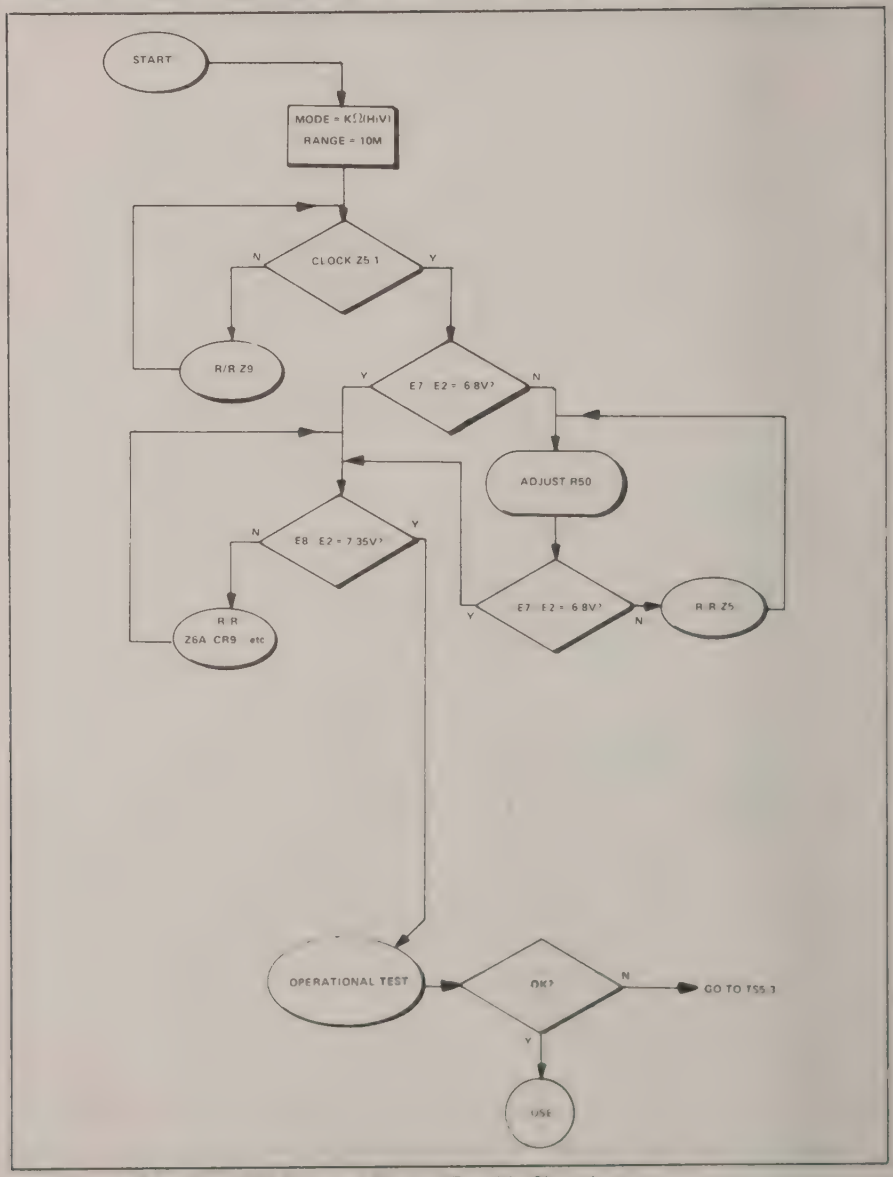

Figure 5-4. Test TS5-2, Power Supply Trouble Shooting

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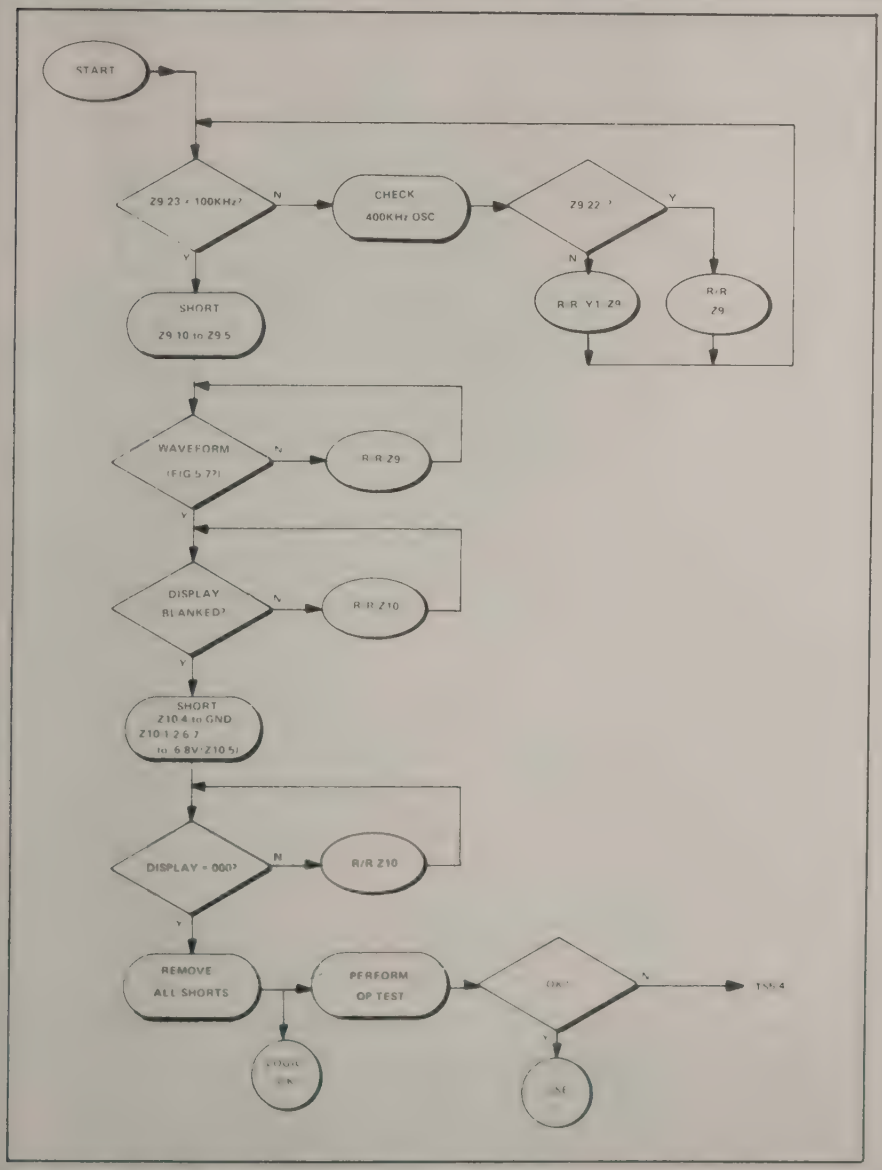

Figure 5-5. Test TS5-3, Digital Logic Trouble Shooting

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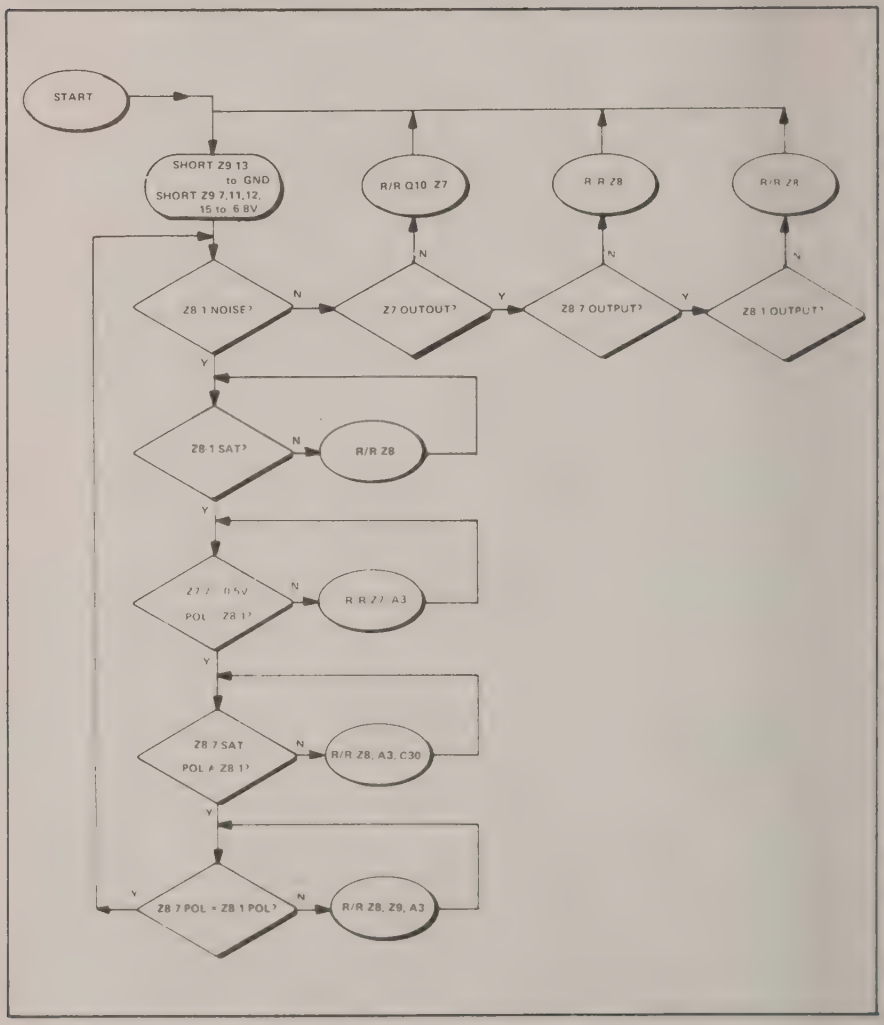

Figure 5-6. Test TS5-4, Analog A/D Trouble Shooting

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Chapter 6
PARTS LISTS

6.1 MAIN ASSEMBLY

REF DESIG	DESCRIPTION	DP PART NO.
A1	RESISTOR NETWORK, INPUT ATTENUATOR	22-48-1085-01
A2	RESISTOR NETWORK, KΩ VOLTAGE SOURCE	22-48-1071
A3	RESISTOR NETWORK, A/D CONVERTER	22-48-1062
A4	RESISTOR NETWORK, POWER SUPPLY	22-48-1072
A5	RESISTOR NETWORK, 680Ω, 6 PIN SIP, 2%	22-721003
A6, 7	RESISTOR NETWORK, 150Ω, 8 PIN SIP, 2%	22-731008
A8	RESISTOR NETWORK, 150Ω, 6 PIN SIP, 2%	22-721002
C1-2	CAPACITOR, 15 pF, 3KV, 5%, DISC, NOP	23-112001
C3	CAPACITOR, 68 pF, 1KV,10%, DISC	23-110019
C4, 5, ..., 48	CAPACITOR, 10-60 pF, TRIM, TOP ADJ	23-810008
C49	CAPACITOR, 1000 pF, DM10, 5%, MICA	23-311002
C50, 52	CAPACITOR, FSV, EDPU 4 x 4 DISC	
C51	CAPACITOR, 0.015 µF, 50V, 2%, POLYSTY	23-[illegible].01
C54, 55	CAPACITOR, 68 µF, 15V, 20%, TANT	23-442004
C56	CAPACITOR, 51 pF, DM10 (FSV OPTL)	23-310016
C57, 58	CAPACITOR, 0.15 µF, 50V, 2%, POLYCARB	23-[illegible]14
C59	CAPACITOR, 150 pF, DM10, 5%, MICA	23-31[illegible]
C60, 61	CAPACITOR, 270 pF, 1KV, 10%, DISC	23-11[illegible]
C62	CAPACITOR, 0.1 µF, 12V, 20%, DISC	23-118206
C63, 64	CAPACITOR, 15 µF, 10V, 20%, TANT	23-441003
C65	CAPACITOR, 4.7 µF, 35V, 20%, TANT	23-441052

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REF. SYMBOL	DESCRIPTION	D. P. P.
C19	CAPACITOR, 3.3 µF, 16V, 20%, TANT. EL.	23-441007
C20, 26, 27	CAPACITOR, 0.01 µF, 150V, +60% -40%,Z5V	23-111006
C21, 30	CAPACITOR, 1 µF, 50V, 10%, POLYCARB	23-510001
C23	CAPACITOR, 0.056 µF, 50V, 10%, POLYCARB	23-510020
C25	CAPACITOR, 0.22 µF, 50V, 5%, POLYCARB	23-510017
C28	CAPACITOR, 47 µF, 6.3V, 20%, TANT. EL.	23-441053
C29, 32	CAPACITOR, 10 pF, 1KV, 10%, CERM.	23-110003
C31	CAPACITOR, 1.0 µF, 50V, 20%, CERM.	23-142000
C34, 38, 40, 41, 43, 44	CAPACITOR, 100 µF, 10V, 20%, ALUM. EL.	23-620006
C36	CAPACITOR, pF, 1KV, 10%, DISC	23-110014
C37	CAPACITOR, 2500 µF, 16V +50% -10% AL.EL.	23-620005
C39	CAPACITOR, 0.001 µF, 500V, 10%, DISC	23-111005
C42	CAPACITOR, 1 µF, 35V, 20%, TANT. EL.	23-441001
C45, 48, 56	CAPACITOR, 6.8 µF, 20V, 20%, TANT. EL.	23-441005
C52	CAPACITOR, .0015 µF, 600V, 10%, DISC.	23-110055
C53	CAPACITOR, .022 µF, 1KV, MYLAR	[illegible]
C54	CAPACITOR, 910 pF, 500V, 5%, DM15	23-311027
C3	CAPACITOR, 68 pF, 5%, DM10, MICA	23-310019
C6, 50	CAPACITOR, FSV, 5%, DM10, MICA	
CR1	DIODE, IN4007	24-104007
CR2	DIODE, IN963B, ZENER, 12V	24-120094
CR3-6	DIODE, A14U, RECT, 2.5A, 25V PIV	
CR7, 8	DIODE, IN4004	24-[illegible]
CR9	DIODE, ZENER, REF, 6.2 - 6.4V	24-48-1001
CR10, 12, 15, 16	DIODE, IN4148, SILICON	24-[illegible]
CR13, 14	DIODE, ZENER, IN4734A	24-[illegible]

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REF. SYMBOL	DESCRIPTION	D. P. P/N
P3	CONNECTOR, FLEX, 12 PIN	25-690076
P4	CONNECTOR, FLEX, 17 PIN	25-690077
P1, 2	CONNECTOR, FLEX, 21 PIN	25-690075
L1	INDUCTOR, 100 µH,	25-100101
Q1-3	TRANSISTOR, MPS-A92, PNP, SILICON	24-240A92
Q4,7,8,10,12,13,14,25	TRANSISTOR, FET N CHAN, YEL/WHT	24-48-1014-09
Q6, 19-24	TRANSISTOR, 2N5818, NPN, SILICON	24-235818-A
Q9, 16, 17	TRANSISTOR, FET N CHAN, YEL/GRN	24-48-1014-07
Q11	TRANSISTOR, FET P CHAN, RED	24-38-1046-01
Q18	TRANSISTOR, 2N5819, PNP, SILICON	24-245819-A
Q5	TRANSISTOR, D40D2, NPN, POWER	24-2240D2
Q15	TRANSISTOR, FET N CHAN, WHT	24-48-1074-02
R1	RESISTOR, 2.2 MEG, 1/8W, 5%, C,	22-012259
R2, 38	RESISTOR, 270K, 1/4W, 5%, C.	22-022749
R3	RESISTOR, 7.5M, 1/4W	22-027559
R4, 5, 36	RESISTOR, 270K, 1/2W,	22-032749
R6	RESISTOR, FSV, 1/8W,	
R7	RESISTOR, 1.6K, 1/4W, 5%, C.	22-021629
R8	RESISTOR, 330K, 2W, 5%, C.C.	22-053249-A
R9	RESISTOR, 100Ω, 1/4W, 5% C.	22-021 1[illegible]
R11	RESISTOR, 18K, 1/4W, 5% (FSV OPTL)	22-021834
R12	RESISTOR, 6.8K, 1/4W, 5%, C.	22-026824
R19	RESISTOR, 10K, TRIM, 20%	22-[illegible]
R1[illegible]	RESISTOR, 8.66K, 1%, RN55C	22-[illegible]
R22	RESISTOR, 2.7Ω, 1/4W, 5%, C.	22-[illegible]
R26, 34	RESISTOR, 1K, 1%, RN55C	22-[illegible]

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REF. SYMBOL	DESCRIPTION	D. P. P/N
R19, 22	RESISTOR, 100K, TRIM, 20%	22-666104
R20	RESISTOR, 2.2M, 1/4W, 5%, C.	22-022259
R21, 33, 48	RESISTOR, 68K, 1/4W, 5%, C.	22-026839
R23	RESISTOR, 33Ω, 1/4W, 5%, C.	22-023309
R25	RESISTOR, 500Ω, TRIM, 20%	22-666501
R26	RESISTOR, 10.0K, 1%, RM55C	22-341002
R27	RESISTOR, 250Ω, TRIM, 20%	22-666251
R28	RESISTOR, 910Ω, 5%, +3500ppM ±10%	22-269119
R29	RESISTOR, 332Ω, 1%, RN55C	22-343320
R30	RESISTOR, 75K, 1/4W, 5%, C.	22-027539
R31, 32	RESISTOR, 300Ω, 1/4W, 5%, C.	22-023019
R35, 64, 65	RESISTOR, 15K, 1/4W, 5%, C.	22-021539
R37	RESISTOR, FSV, 1/4W, C. (FSV)	
R10, 39, 43, 44	RESISTOR, 100K, 1/4W, 5%, C.	22-021049
R41	RESISTOR, 2.2M, 1/8W,	22-012259
R42	RESISTOR, 7.5K, 1/8W,	22-017529
R45	RESISTOR, 22Ω, 1/2W,	22-032209
R46	RESISTOR, 1K, 1/4W,	22-021029
R47	RESISTOR, 6.8Ω, 1/4W,	22-026R89
R49	RESISTOR, 22K, 1/4W, 5%, C.	22-022239
R50, 53	RESISTOR, 2.5K, TRIM, 20%	22-666252
R51	RESISTOR, 4.87K, 1%, RN55C	22-344871
R52	RESISTOR, 1.24K, 1%, RN55C	22-341241
R54, 61, 40	RESISTOR, 10Ω, 1/4W, 5%, C.	22-021009
R55	RESISTOR, FSV, 1%, RN55C	
R56	RESISTOR, 59.0K, 1% RN55C	22-345902
R57	RESISTOR, 499Ω, 1%, RN55C	22-344990
R58	RESISTOR, 205Ω, 1%, RN55C	22-342050
R[illegible]	RESISTOR, 301Ω, 1%, RN55C	22-343010
R[illegible]2	RESISTOR, 2.2K, 1/4W, 5%, C.	22-022229
R[illegible]	RESISTOR, 27K, 1/4W, 5%, C.	22-022739

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REF. SYMBOL	DESCRIPTION	D. P. P/N
R13	RESISTOR, 470K, 2W, 10%, C.	22-054748
R16	RESISTOR, 900Ω (ITEM 1) 0.25%	22-48-1068-01
R17 ASSEMBLED	RESISTOR, 90Ω (ITEM 2) 0.25%	22-48-1068-02
R34 ON SWITCH	RESISTOR, 9Ω (ITEM 3) 0.25%	22-48-1068-03
R[illegible] S1 (ITEM 151)	RESISTOR, 0.9Ω (ITEM 4) 0.25%	22-48-1068-04
R[illegible]	RESISTOR, 0.1Ω (ITEM 5) 0.25%	22-48-1068-05
S1	SWITCH, PUSHBUTTON, 17 STATION	D68-1011
T1	TRANSFORMER, POWER	C68-1012-02
Y1	RESONATOR, CERAMIC	25-141000
Z1	INT. CKT., DUAL OP AMP, NE532V	24-400532
Z2, 7	INT. CKT., OP AMP, LF356H	24-420356-01
Z3	INT. CKT., TRUE RMS CONV., 3737	24-303737
Z4, 8	INT. CKT., DUAL COMP., LM393	24-400393
Z5	INT. CKT., SWITCHING REG., TL497CN	24-380497
Z6	INT. CKT., DUAL OP AMP, 1458	24-405558
Z9	INT. CKT., LSI CMOS A/D LOGIC	24-48-1058
Z10	INT. CKT., DECODER/DRIVER, MC14511	24-L14511

6.2 DISPLAY ASSEMBLY

Flex Cable Assembly (normal Brightness) 60-1027
Display Card Assembly (High Brightness) 60-1042

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6.3 BCD OUTPUT OPTION

REF DESIG	DESCRIPTION	DP PART NO.
A201, 203, 205	RESISTOR NETWORK, 10,, 6 PIN SIP	22-72001
A202	RESISTOR NETWOPK, 1K, 8 PIN SIP	22-731005
A204	RESISTOR NETWORK, 100K, 6 PIN SIP	22-720002
A206	RESISTOR NETWORK, 47K, 8 PIN SIP	22-731006
A207	RESISTOR NETWORK,4.7K, 8 PIN SIP	22-731007
C201	CAPACITOR, 0.22 µF, 35V, TANT, 20%	23-44105
C202-205	CAPACITOR, 3300 pF, 50V, CERM.	23-14004
CR201-204	DIODE IN4148	24-110001
CR205-208	DIODE IN270	24-140270
Q201	TRANSISTOR 2N3906	24-243906
Q202	TRANSISTOR, FET, YEL/GRN	24-48-1014-07
Q203-206	TRANSISTOR 2N3904	24-233904
R201, 205, 208	RESISTOR, 1K, 1/4W, 5%	22-021029
R202	RESISTOR, 62K	22-026239
R203	RESISTOR, 2K	22-022029
R204, 206	RESISTOR, F.A.	22-02***9
R209	RESISTOR, 200K, 1/4W, 5%	22-[illegible]
T201	TOROID MODULE	B68-101*
Z201	I.C. 74C157	24-G74C157
Z202, 206	I.C. 4013	24-104013
Z203-205	I.C. ILQ-74	24-MILQ74
Z[illegible]	I.C. [illegible]	24-G74[illegible]
Z[illegible]	I.C. 4[illegible]	24-114[illegible]

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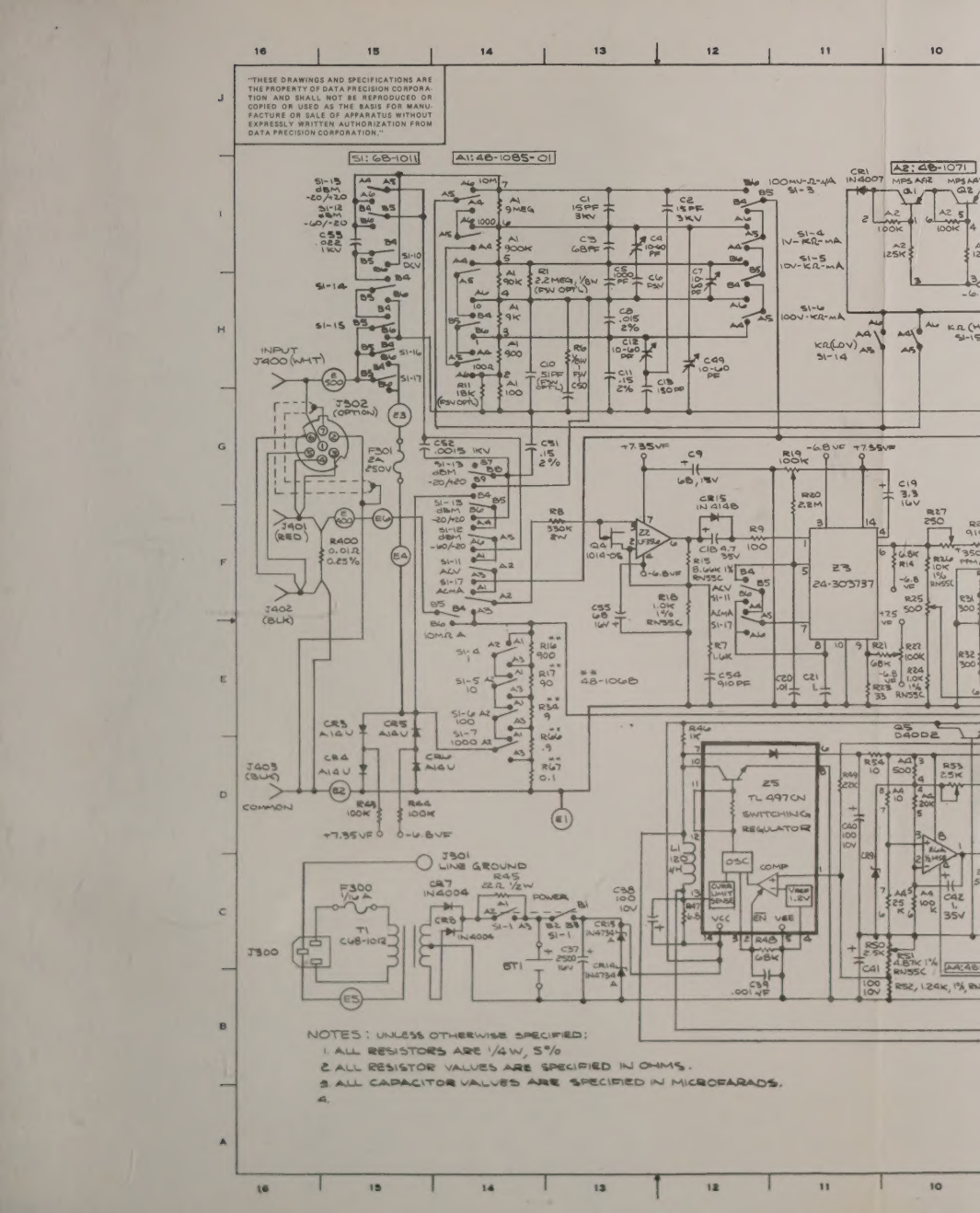
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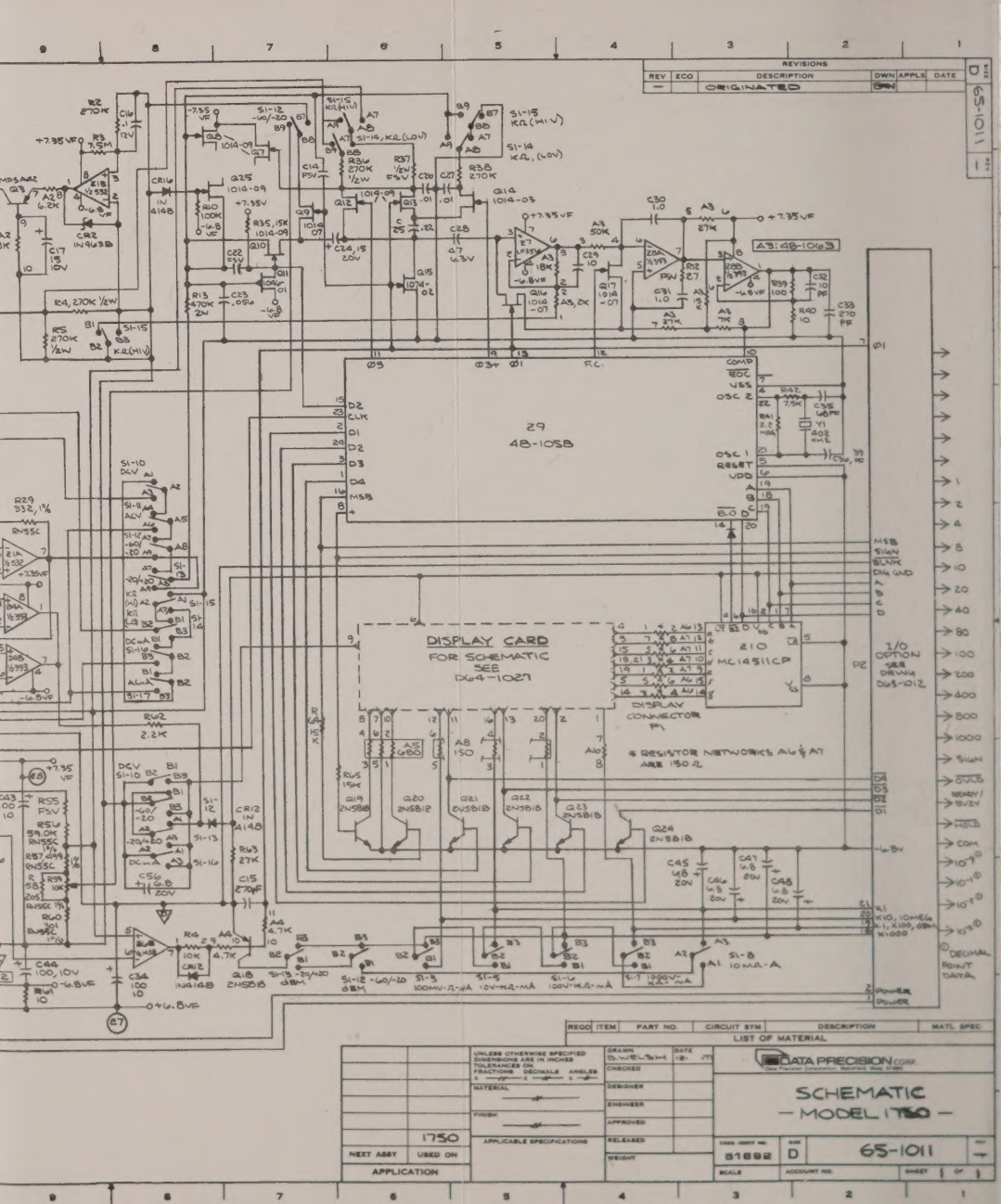
A1: 48-1085-01
A2: 48-1071
INPUT J400 (WHT)
J401 (RED)
J402 (BLK)
J403 (BLK) COMMON
J300
J301 LINE GROUND
J302 (OPTION)
F300 1/10 A
F301 2A 250V
T1 C48-1012
Z3 24-305737
Z5 TL 497CN SWITCHING REGULATOR
OSC
COMP
VREF 1.2V
+7.35VF
-6.8VF
NOTES: UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTORS ARE 1/4W, 5%
2. ALL RESISTOR VALUES ARE SPECIFIED IN OHMS.
3. ALL CAPACITOR VALUES ARE SPECIFIED IN MICROFARADS.
4.


REVISIONS
REV. ECO DESCRIPTION DWN APPD'S DATE
— ORIGINATED BW
65-1011
DISPLAY CARD
FOR SCHEMATIC
SEE
D64-1027
DISPLAY CONNECTOR P1
* RESISTOR NETWORKS A6 & A7 ARE 150 Ω
I/O OPTION SEE DRWG D65-1012
LIST OF MATERIAL
REQD ITEM PART NO. CIRCUIT SYM DESCRIPTION MATL SPEC
DATA PRECISION CORP.
SCHEMATIC
— MODEL 1750 —
1750
NEXT ASSY USED ON
APPLICATION
81892 D 65-1011

MP MASTER
MA28643

DATA PRECISION
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